

Starlord KBL_Refresh Schematics KabyLake-R

2017-05-25

REV : A00

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DY : None Installed

UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

Starlord KBLR DIS BBY U42



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A3

Document Number

Starlord KBL-R

Rev

A00

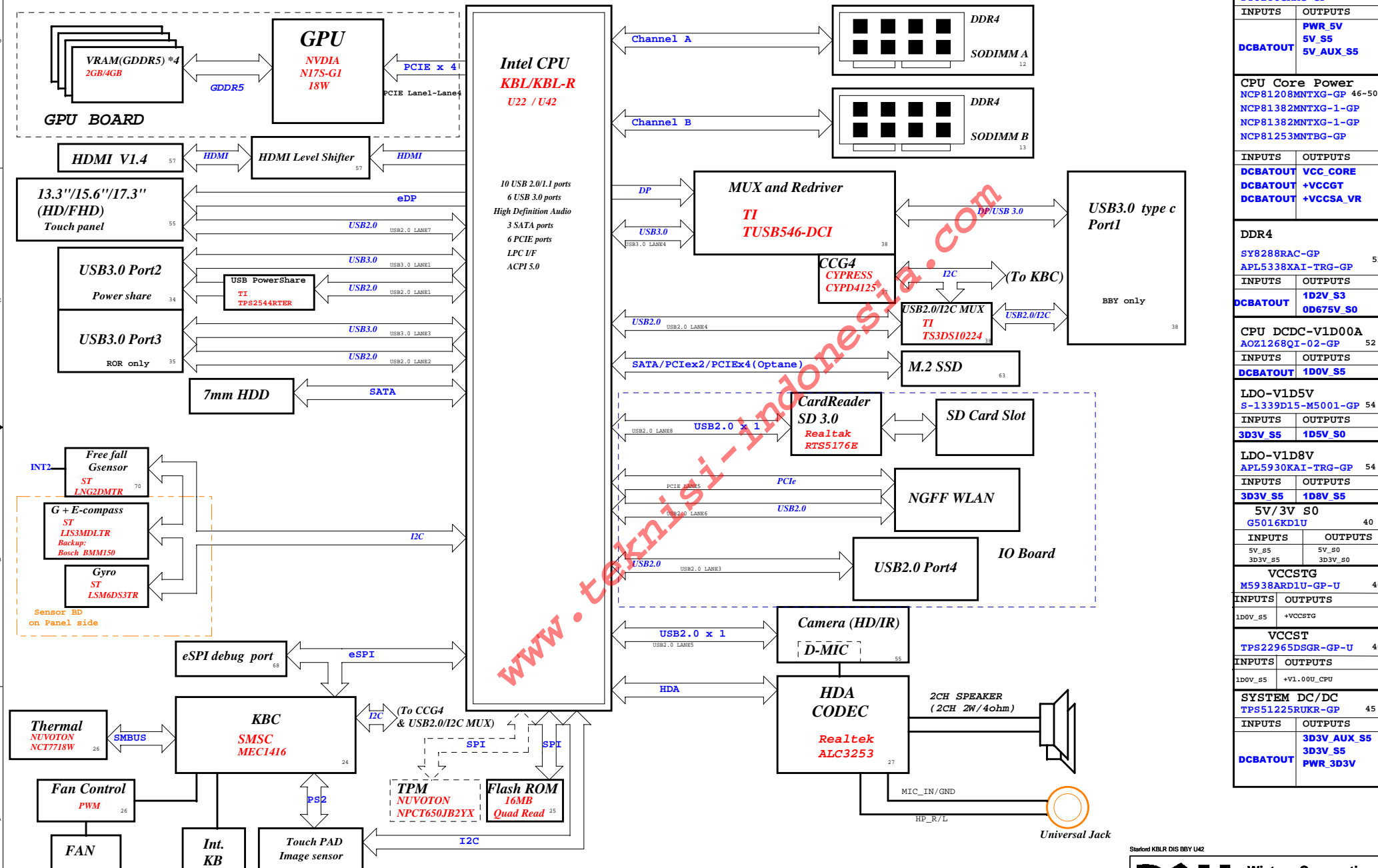
Date: Friday, June 30, 2017

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Star lord KBL Block Diagram

Revision: A00

	SENSOR	IO	MB
ROR	17A18-SA	17A17-SA	17810-1
BBY	17A18-SA	17A16-SA	16888-1



CHARGER ISL88739		44
INPUTS	OUTPUTS	
AD+ BT+	DCBATOUT	
SYSTEM DC/DC SY8288CRAC-GP		
INPUTS	OUTPUTS	
DCBATOUT	PWR_S5 5V_S5 5V_AUX_S5	
CPU Core Power NCP81208MNTXG-GP		
NCP81382MNTXG-1-GP		
NCP81382MNTXG-1-GP		
NCP81253MNTBG-GP		
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
DCBATOUT	+VCCGT	
DCBATOUT	+VCCSA_VR	
DDR4 SY8288RAC-GP		
APL5338XAI-TRG-GP		
INPUTS	OUTPUTS	
DCBATOUT	1D2V_S3 0D67V_S0	
CPU DCDC-V1D00A AOZ1268QI-02-GP		
INPUTS	OUTPUTS	
DCBATOUT	1D0V_S5	
LDO-V1D5V S-1339D15-M5001-GP		
INPUTS	OUTPUTS	
3D3V_S5	1D5V_S0	
LDO-V1D8V APL5930KAI-TRG-GP		
INPUTS	OUTPUTS	
3D3V_S5	1D8V_S5	
5V/3V_S0 G5016KD1U		
INPUTS	OUTPUTS	
5V_S5 3D3V_S5	5V_S0 3D3V_S0	
VCCSTG M5938ARD1U-GP-U		
INPUTS	OUTPUTS	
1D0V_S5	+VCCSTG	
VCCST TPS22965DSGR-GP-U		
INPUTS	OUTPUTS	
1D0V_S5	+V1.00U_CPU	
SYSTEM DC/DC TPS51225KRKG-GP		
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5 3D3V_S5 PWR_3D3V	

Starlord KBLR DIS BBY U42



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Title				Block Diagram			
Size	Document Number					Rev	
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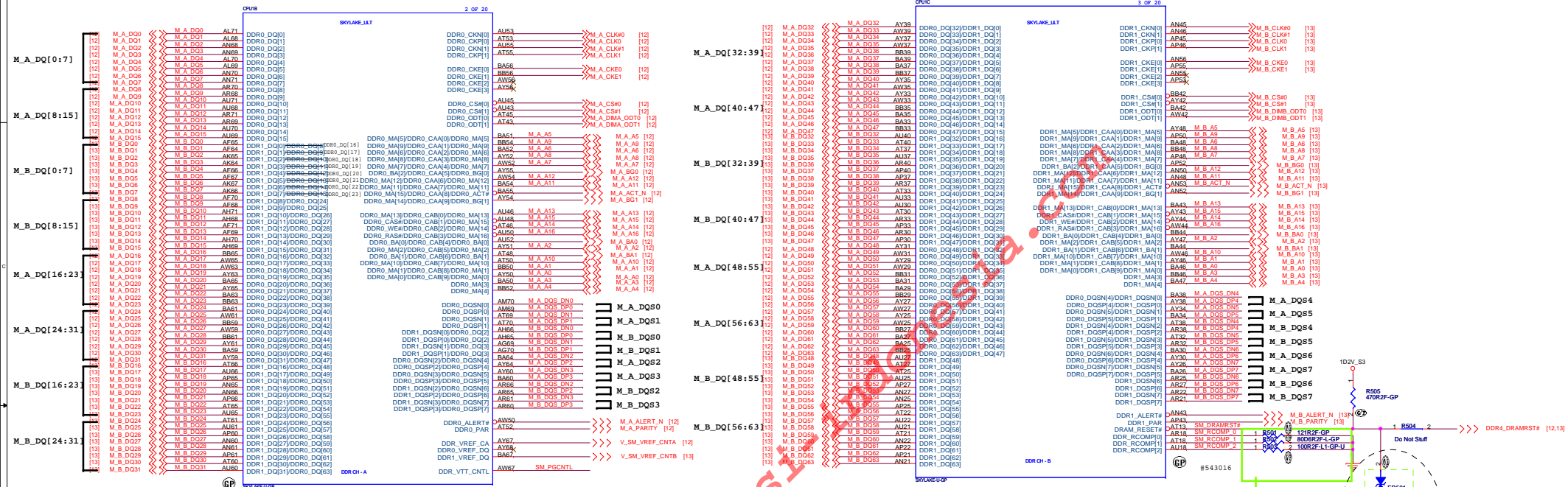
SSID = CPU

(Blanking)

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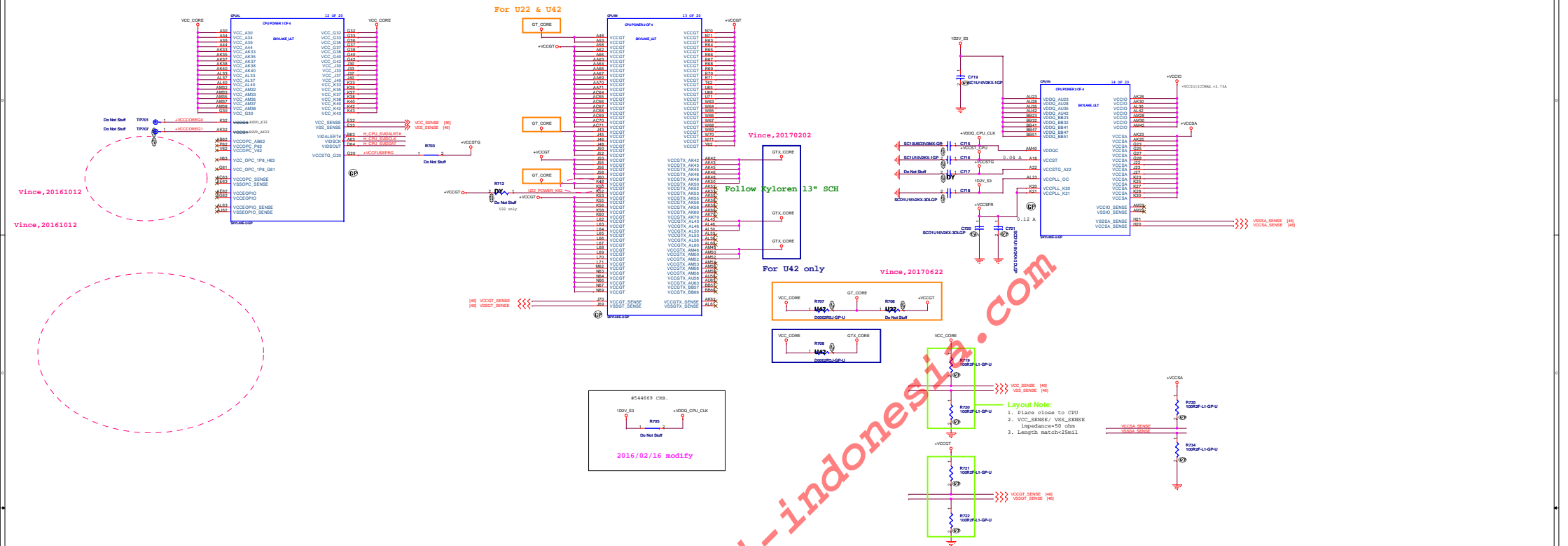
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Title (Reserved)			
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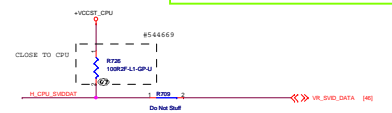


Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

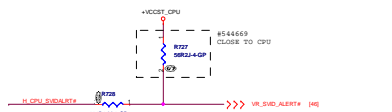
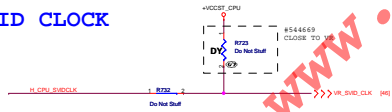


SVID DATA

Layout Note:
The total length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.



SVID CLOCK



SVID_543016:

Figure 10-7. Routing Illustration for SVID Topology

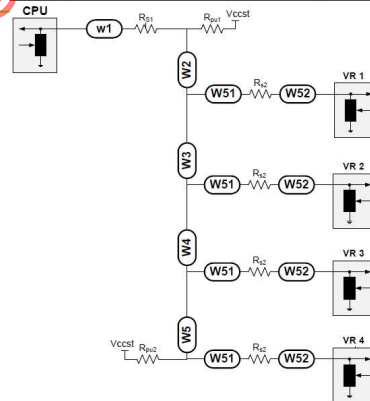


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W1 [inches]	W2 [inches]	R _{pull} [Ω]	C _{pull} [pF]	R ₁ [Ω]	R ₂ [Ω]	R ₃ [Ω]	R ₄ [Ω]	V _{CC} [V]
VIDSOUT							100	100	0	10			
VIDSCK	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	0	50			1.0
VIDALERT#							56	Empty	220	0			

Standard KBL-R DQS REV 040

Dell Wistron Corporation
21F, 8th, 5th, 1, 2nd, 3rd, 4th, 5th, 6th, 7th, 8th, 9th, 10th, 11th, 12th, 13th, 14th, 15th, 16th, 17th, 18th, 19th, 20th, 21st, 22nd, 23rd, 24th, 25th, 26th, 27th, 28th, 29th, 30th, 31st, 32nd, 33rd, 34th, 35th, 36th, 37th, 38th, 39th, 40th, 41st, 42nd, 43rd, 44th, 45th, 46th, 47th, 48th, 49th, 50th, 51st, 52nd, 53rd, 54th, 55th, 56th, 57th, 58th, 59th, 60th, 61st, 62nd, 63rd, 64th, 65th, 66th, 67th, 68th, 69th, 70th, 71st, 72nd, 73rd, 74th, 75th, 76th, 77th, 78th, 79th, 80th, 81st, 82nd, 83rd, 84th, 85th, 86th, 87th, 88th, 89th, 90th, 91st, 92nd, 93rd, 94th, 95th, 96th, 97th, 98th, 99th, 100th, 101st, 102nd, 103rd, 104th, 105th, 106th, 107th, 108th, 109th, 110th, 111th, 112th, 113th, 114th, 115th, 116th, 117th, 118th, 119th, 120th, 121st, 122nd, 123rd, 124th, 125th, 126th, 127th, 128th, 129th, 130th, 131st, 132nd, 133rd, 134th, 135th, 136th, 137th, 138th, 139th, 140th, 141st, 142nd, 143rd, 144th, 145th, 146th, 147th, 148th, 149th, 150th, 151st, 152nd, 153rd, 154th, 155th, 156th, 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Main Func = CPU

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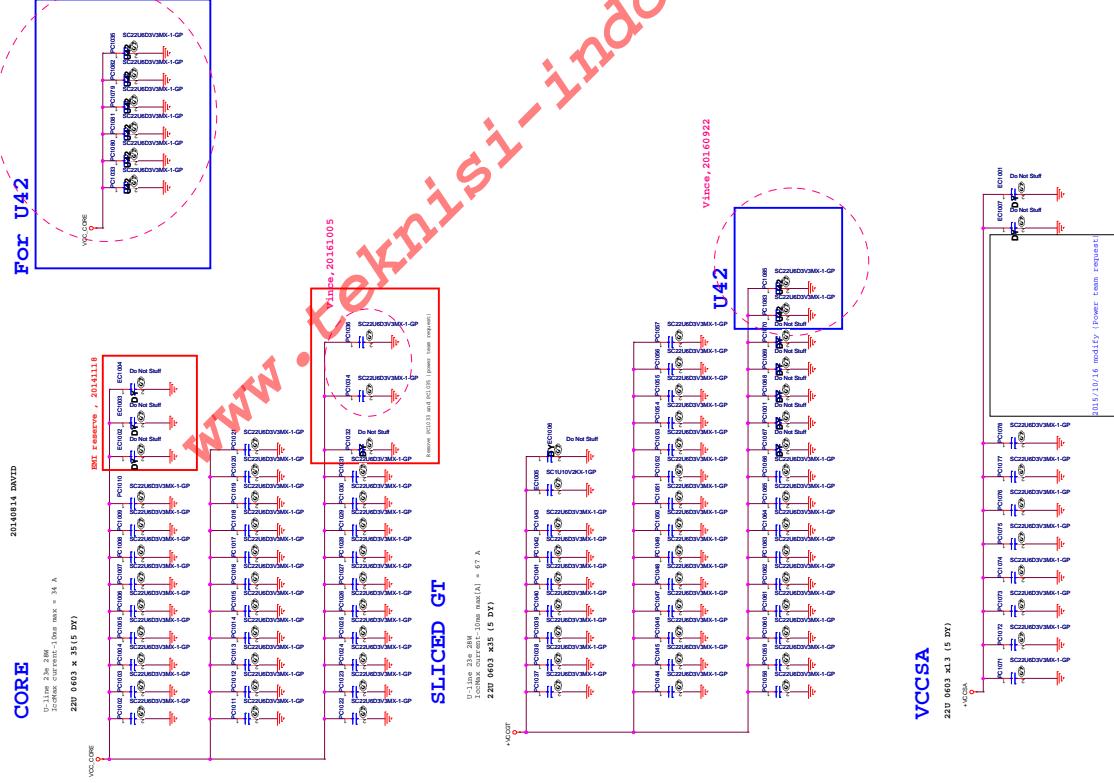
[illegible]

Table 53-3. SKL U Bulk Decoupling Requirements

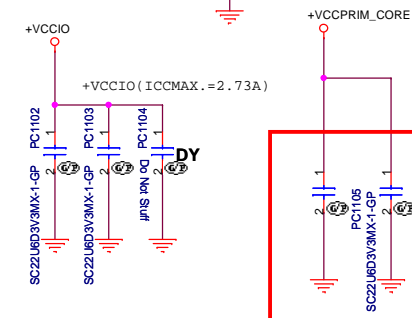
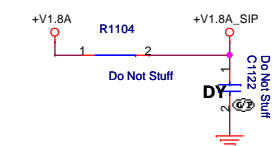
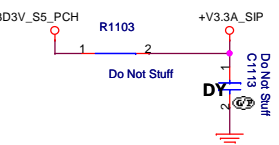
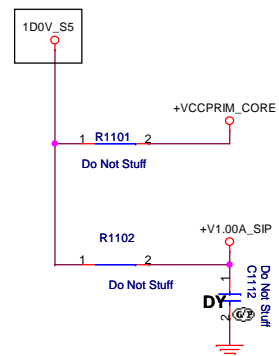
Domain	Backside cap	Primary side ring	Placement guidelines
VCCL	79, 22V 0603	79, 22V 0603	Place on secondary side, underneath the package
VCC	79, 10V 0402	79, 10V 0402	Place on secondary side, underneath the package
	15k, 1uF 0201		
		8x 4V 0603	Place as close to the package as possible
		8x 10V 0402	
VCCGT	10x, 10V 0402		Place on secondary side, underneath the package
	12x, 1uF 0201		
		3x 4V 0603	Place as close to the package as possible
		79, 22V 0603	
		3x 47uF 0005	Place as close to the package as possible
		5x 22uF 0603	Additional components needed when supporting 23e
VCCGTN	8x, 10V 0402		Place on secondary side, underneath the package
			Only needed when supporting 23e
		8x 22uF 0603	Place on secondary side, underneath the package
VCCSA	79, 10V 0402		Place as close to the package as possible
	79, 1uF 0201		
		6x 10V 0402	Place on secondary side, underneath the package
VCCSD	2x, 10V 0402		Place as close to the package as possible
	4x, 1uF 0201		
VDDQ	2x, 10V 0402		Place on secondary side, underneath the package
	4x, 1uF 0201		
		4x, 10V 0402	Place as close to the package as possible
VDDQCC	1x, 1uF 0201		Place on secondary side, underneath the package
VDDQCCN	1x, 1uF 0201		Place on secondary side, underneath the package
VDDQCCS	1x, 1uF 0201		Place as close to the package as possible

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

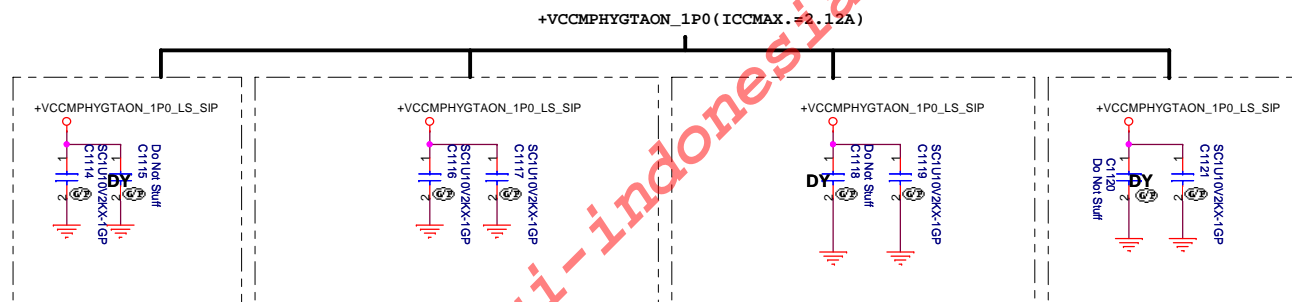
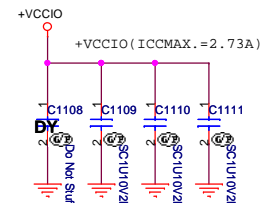
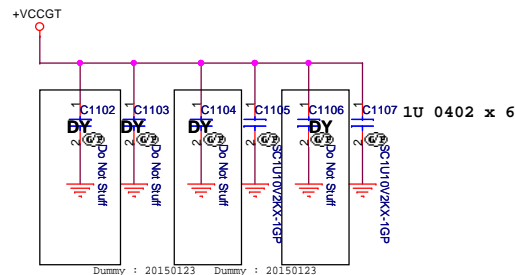
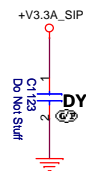
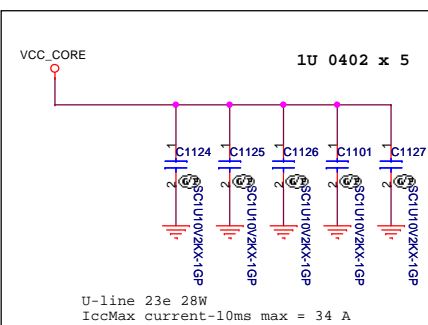
Decoupling	Back-side cap	Primary side cap	Placement guideline
VCC5TG	1x 1uF 0402		Place on secondary side, underneath the package Placeholder only
VCCOEPI0	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 1uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		

Table S3-4. Decoupling Requirements for SKI U Processor (Sheet 2 of 2)

VCCIO



```
Size:0805 change to 0603
20141117
```



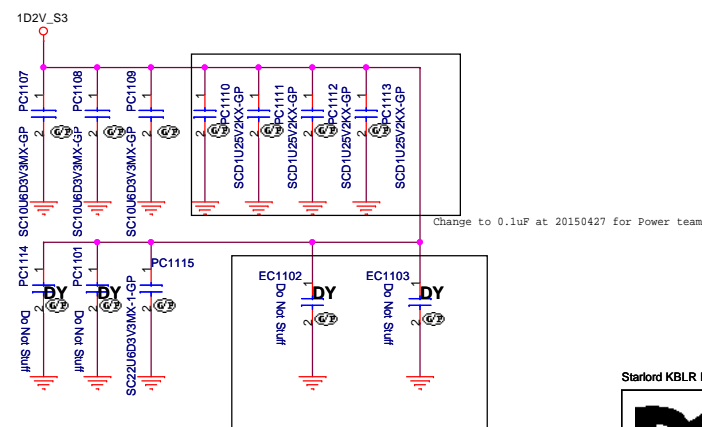
Layout Note:

1uF:

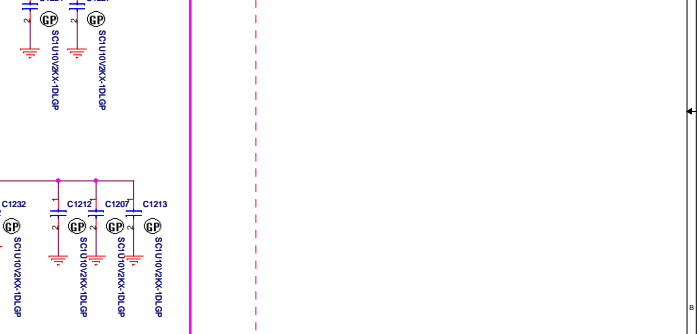
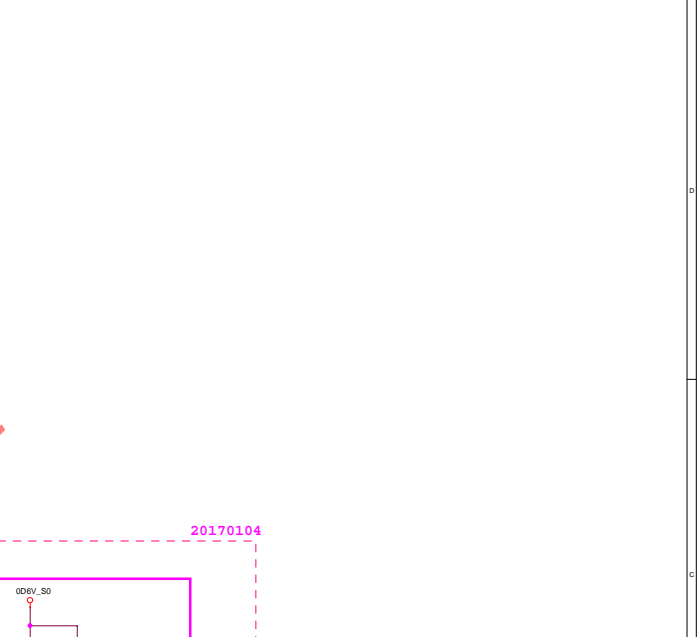
```
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
```

22uF :

C1182 C1184 near N15
10uF:
C1176 near N15




RF request 2016/01/12 modify

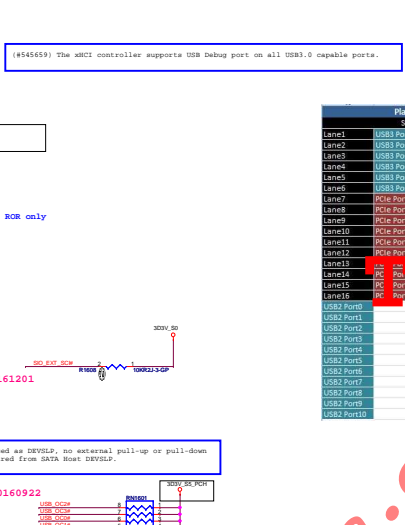


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Title (Reserved)_SODIMM _SODIMM4					
Size A4		Document Number Starlord KBL-R			Rev A00
Date: Friday, June 30, 2017			Sheet 14 of 106		

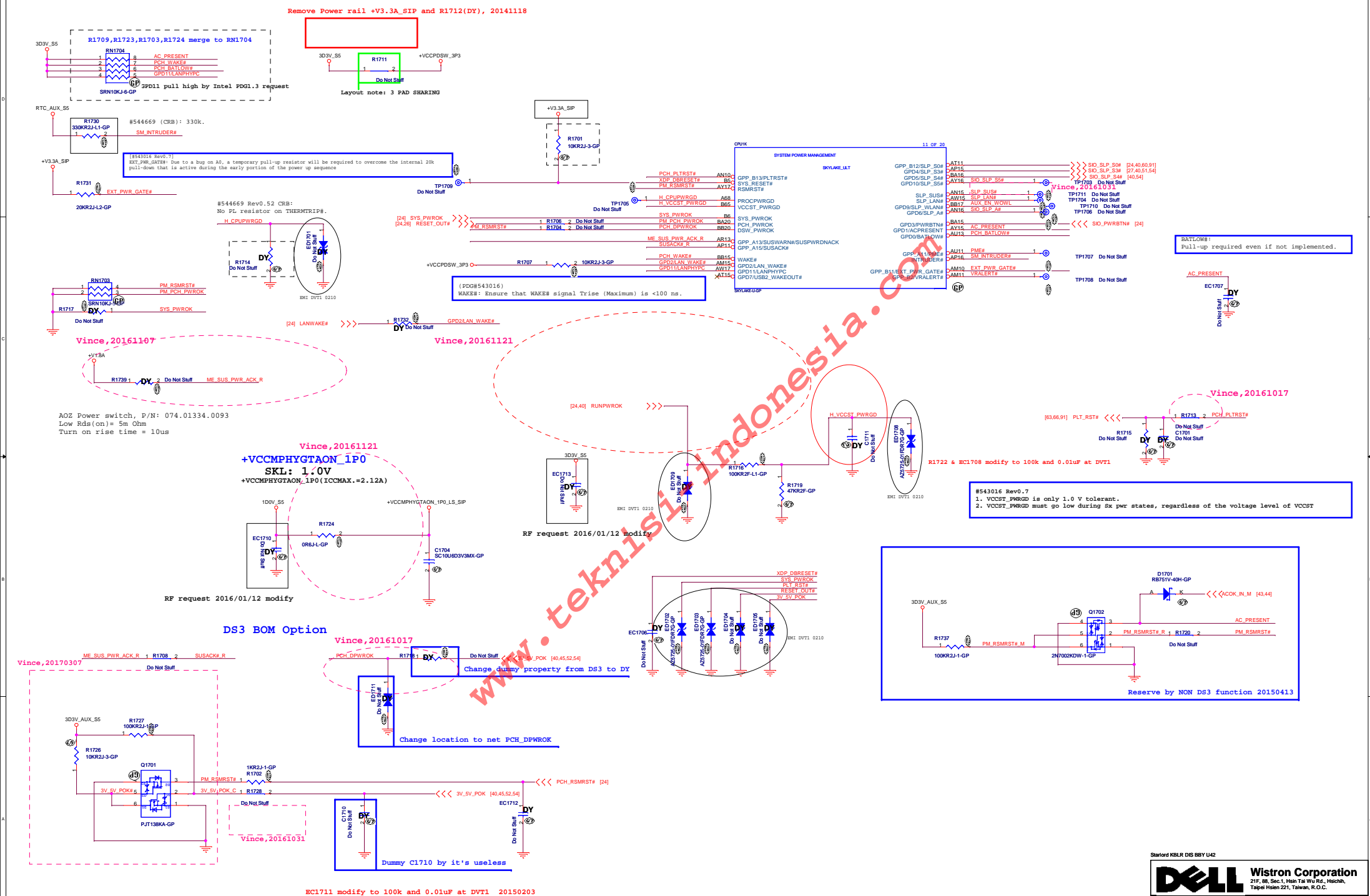


(#543016) Unused SATAGP[2:0]/GPP_E[2:0] pins must be terminated to either 3.3 V rail or GND using 8.2 KΩ to 10 KΩ on the motherboard.
Do not use both pull-up and pull-down. Either pull-up or pull-down is acceptable.

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (M/s)	Theoretical Max Bandwidth (GB/s)			
						x1	x2	x4	
U	6	12	1	8b/10b	2500	0.25	0.50	1.00	
			2	8b/10b	5000	0.50	1.00	2.00	
			3	128b/130b	8000	1.00	2.00	3.94	
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00	
			2	8b/10b	5000	0.50	1.00	2.00	
			3	8b/10b	5000	0.50	1.00	2.00	

SKL	PCIe Link Config	PCI Express* Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3		Port4		Port5		Port7		Port8	
	2x1	Port1		Port2		Port3		Port4		Port5		Port6	
	1x4	Port1				Port5				Port9			
W	1x8	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3		Port4		Port5		Port7		Port8	
	4x1	Port1		Port2		Port3		Port4		Port5		Port6	
	1x2									Port9			
	2x1									Port9		Port10	

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File	
CPU (PCIe/SATA/USB)	
Size A1	Document Number
Starkord KBL-R	
Date	Friday, June 30, 2017
Rev	1.0



PCH strap pin:

PCH strap pin:

PCH Prim

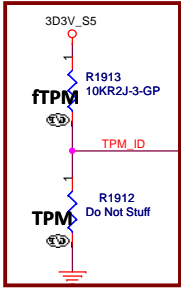
SSID = PCH

Strap pin:

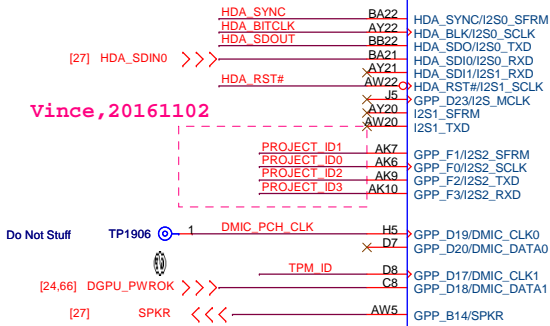
Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. ★ 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. ★ 1 = Port C is detected.

These two signals have weak internal pull-down.

Vince,20161107



Vince,20161102



PCH strap pin:

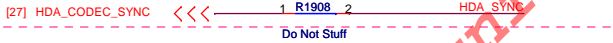
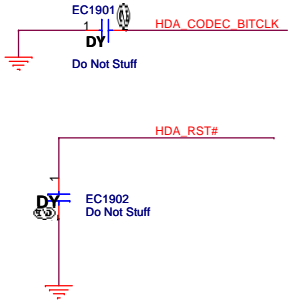
Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDO	Low = Default ★ High = Enable

The internal pull-down is disabled after PLTRST# deasserts

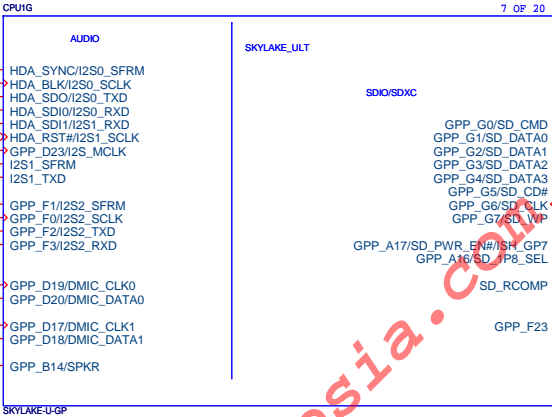
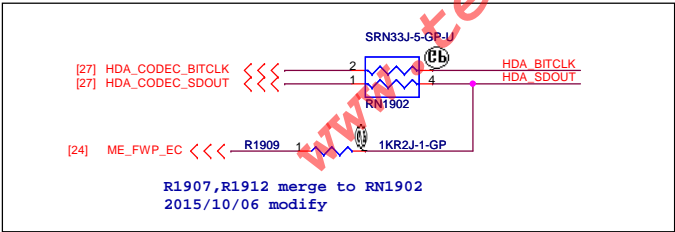
PCH strap pin:

NO REBOOT	
HDA_SPKR	★ Low = Enable (Default) High = Disable

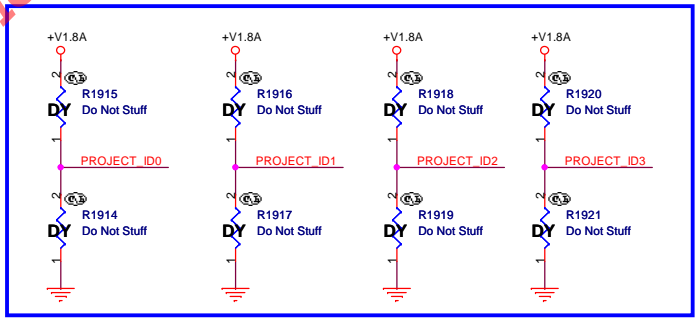
The internal pull-down is disabled after PLTRST# deasserts



Vince,20170106



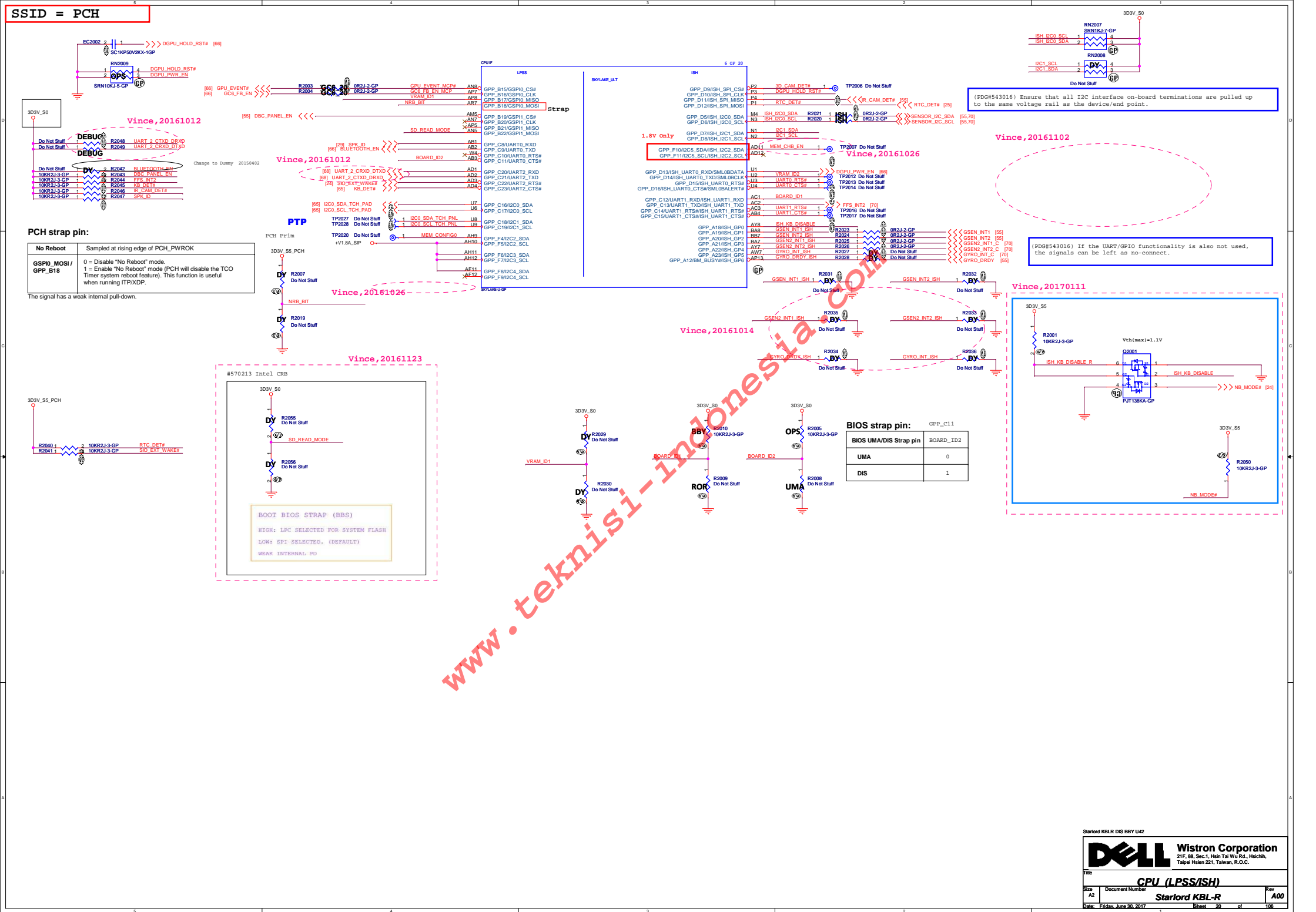
Vince,20170106

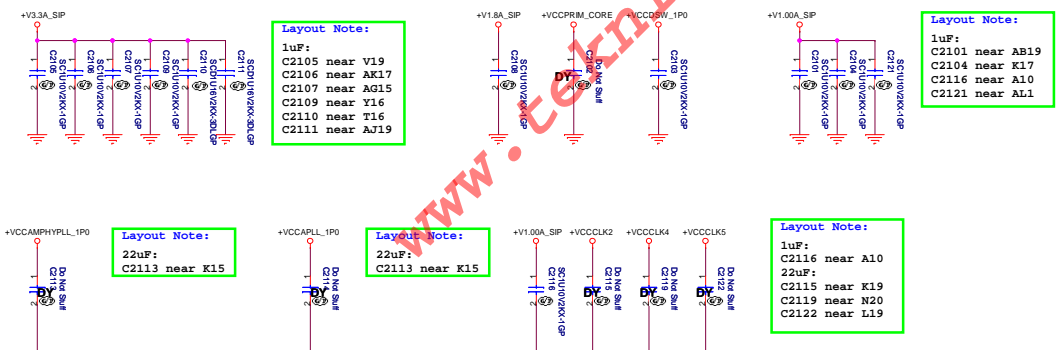


Vince,20161026

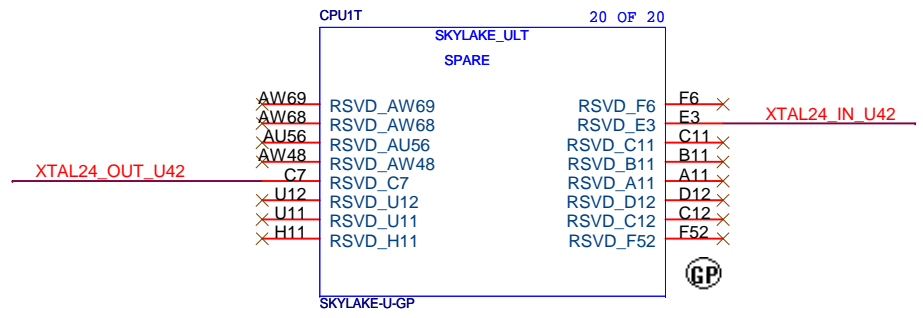
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SSID = PCH

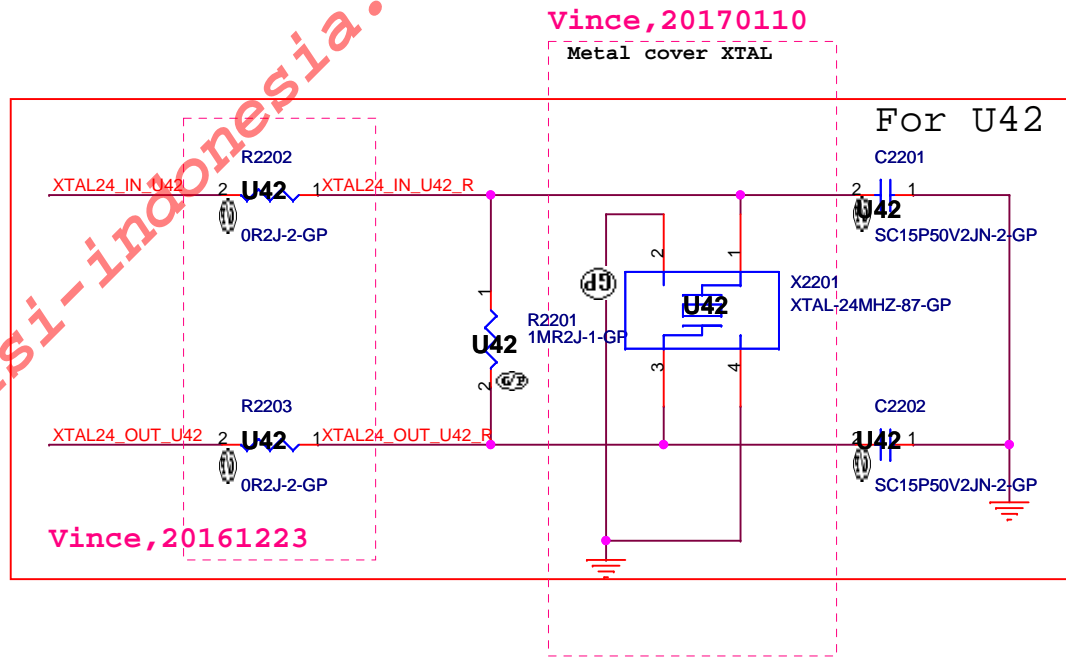




Main Func = PCH



Pin	Connection
#1,#3	X'tal
#2,#4	GND



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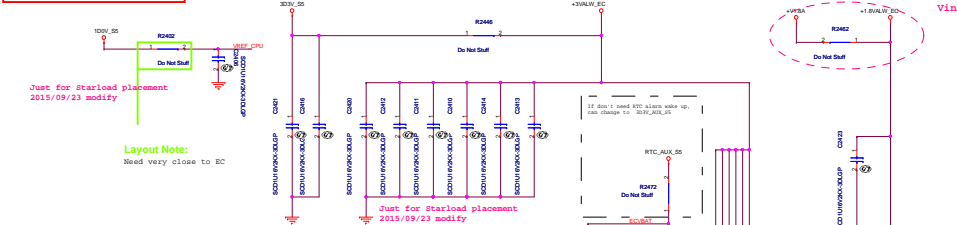
CPU (RSVD)

Size A4	Document Number	Rev A00
Starlord KBL-R		

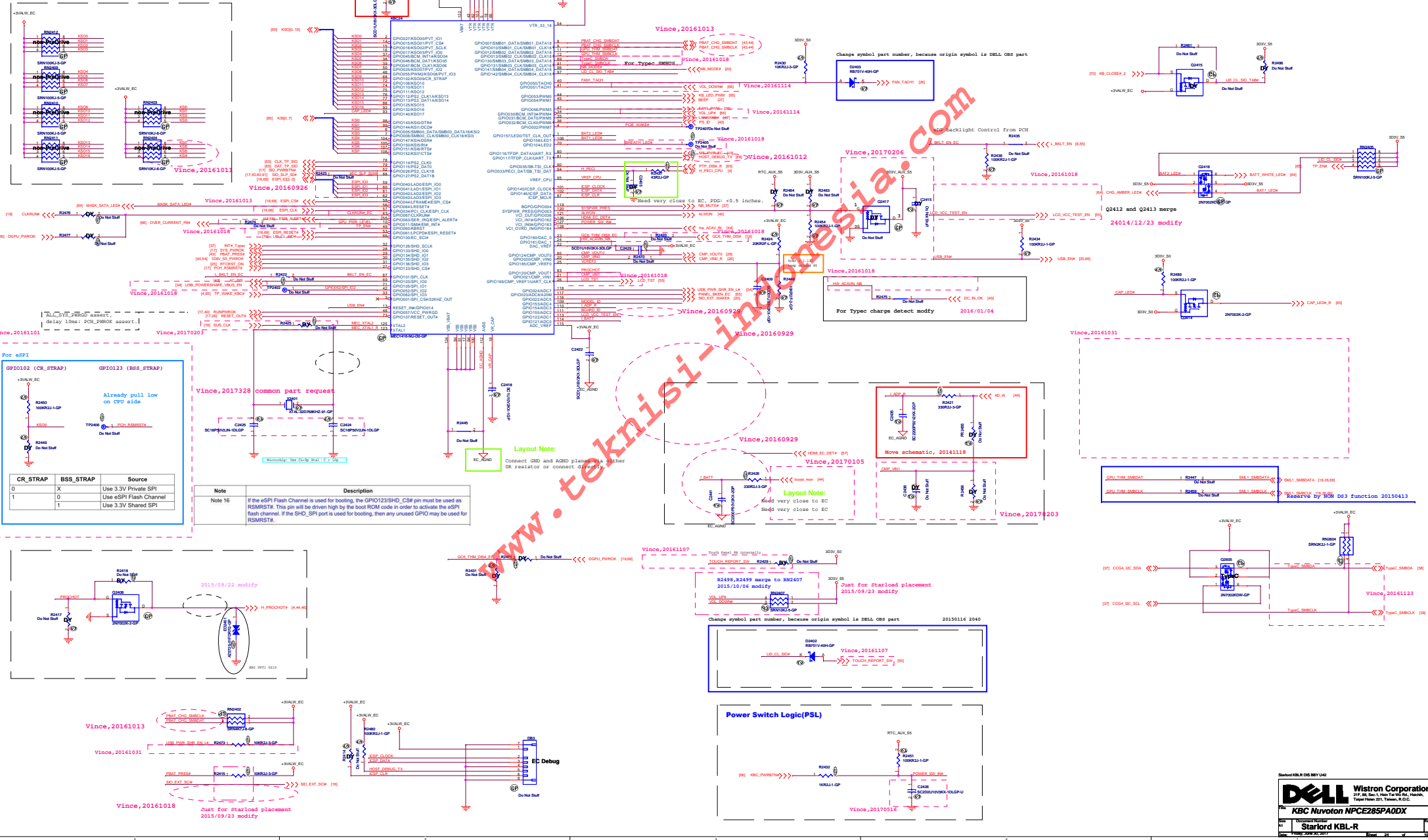
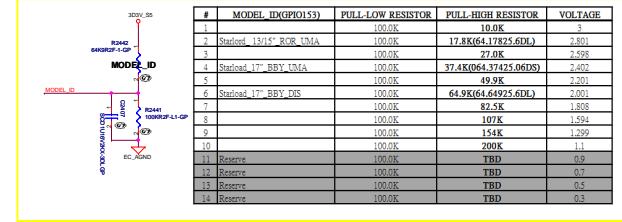
Date: Friday, June 30, 2017

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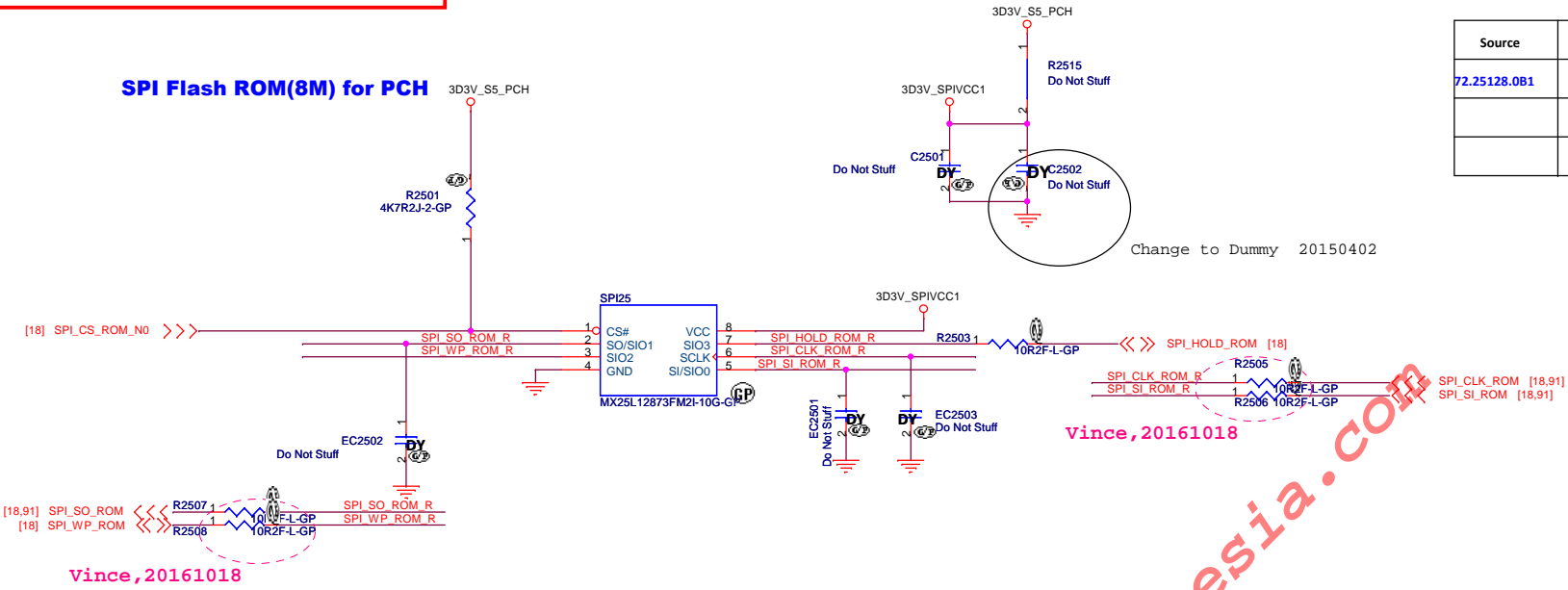
Main Func = KBC



#	Board ID (BP01055)	PULL LOW RESISTOR	PULL HIGH RESISTOR	VOLTAGE
1	X00	100.0K	10.0K	5
2	X01	100.0K	27.0K	2.85
3	X02	100.0K	27.0K	4.58
4	X03 (Internal)	100.0K	37.4K	2.62
5	A00	100.0K	49.9K	2.201
6	A01	100.0K	64.9K	2.001
7	A02	100.0K	82.5K	1.858
8	A03	100.0K	107K	1.68
9	Reserve	100.0K	154K	1.299
10	Reserve	100.0K	200K	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.8
13	Reserve	100.0K	TBD	0.7
14	Reserve	100.0K	TBD	0.5



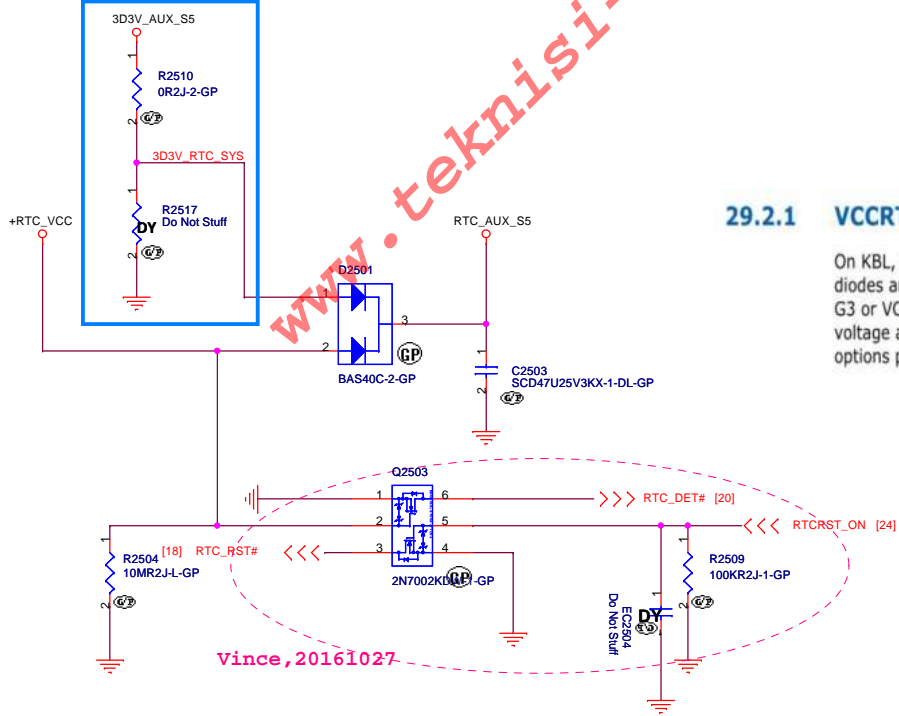
Main Func = SPI Flash



Source	QUAD/DUAL fast read	DUAL fast read	SFDP
72.25128.0B1	O	O	O
	O	O	O
	O	O	O

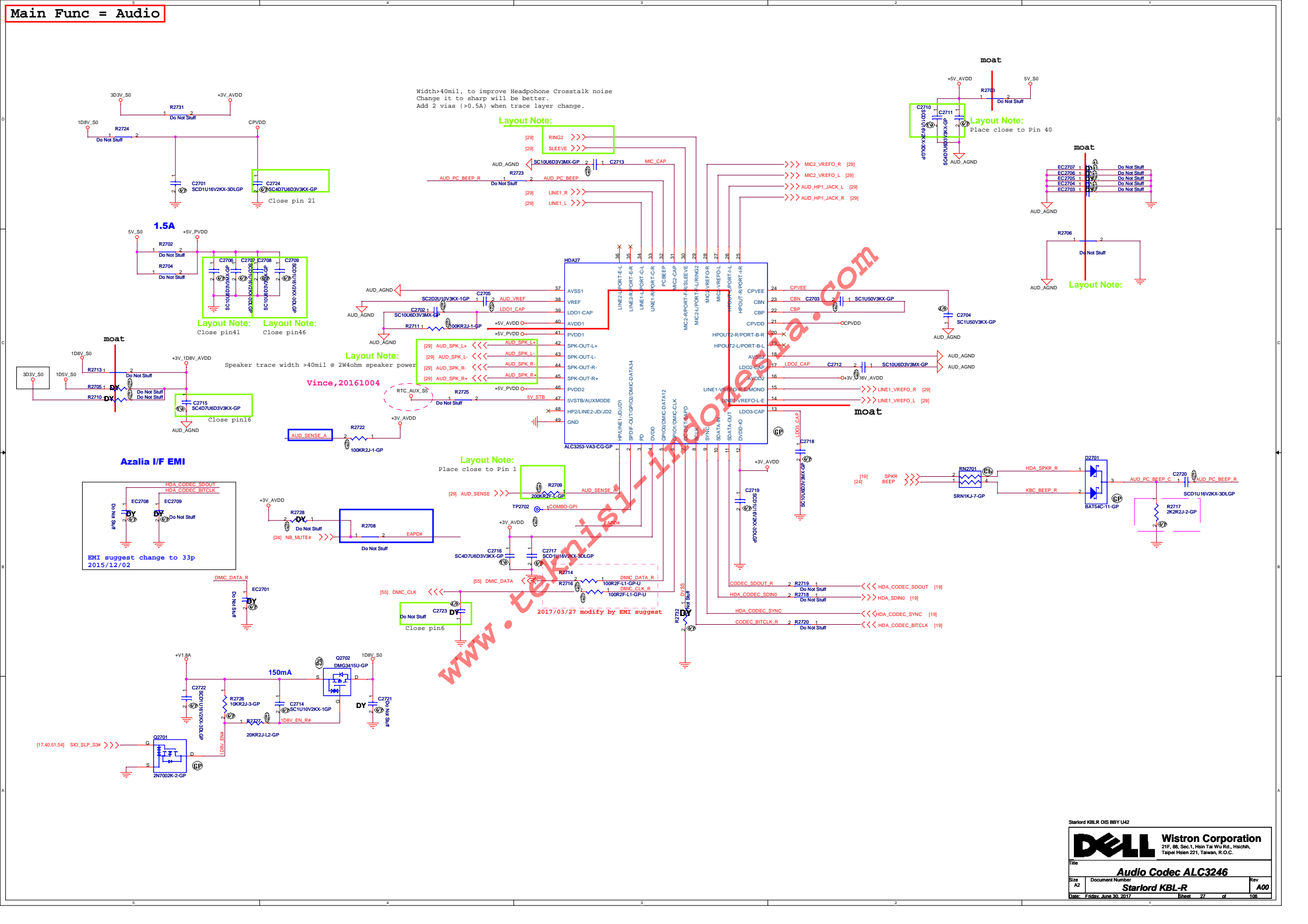
Delivery Voltage 3.19V
(when R2510 1K6 ohm)

Main Func = RTC



29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.



Width>40mil, to improve Headphone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.

Layout Note:

[28] RING2 >>>
[28] SLEEVE >>>
[28] AUD_AGND <<<
[28] AUD_PC_BEEP <<<
[28] LINE1_R >>>
[28] LINE1_L >>>

Layout Note:
Place close to Pin 40

Layout Note:

Layout Note:
Place close to Pin 1

moat

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Main Func = Audio

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SSID = LAN

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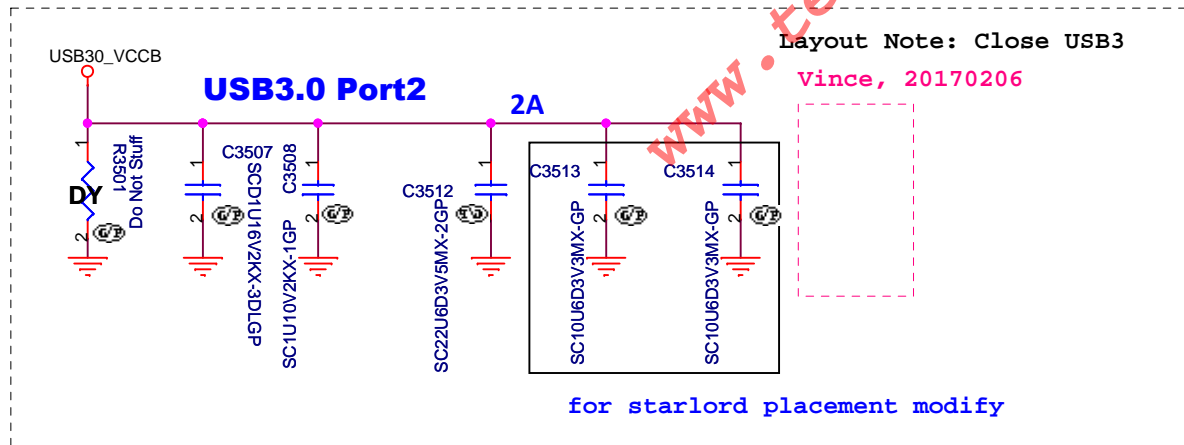
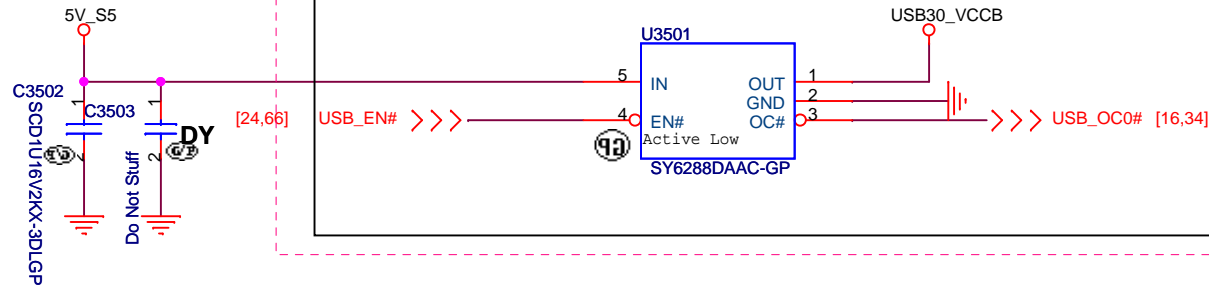
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
XFOM&RJ45			
Size	Document Number		Rev
A3	Starlord KBL-R		A00
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Main Func = USB3.0 Port1

Vince, 20170206



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Title

USB switch

Size

Document Number

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Rev

A00

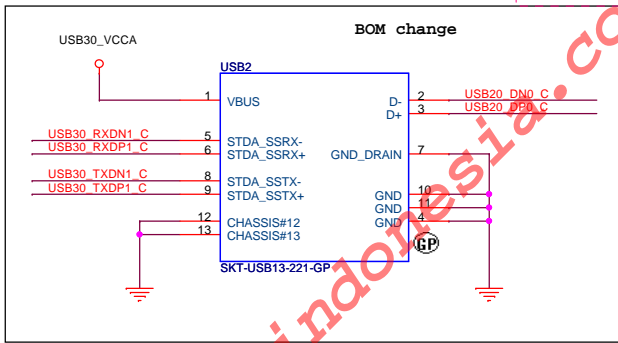
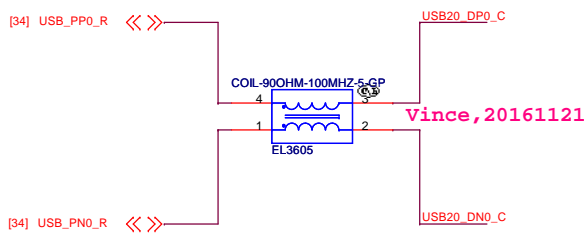
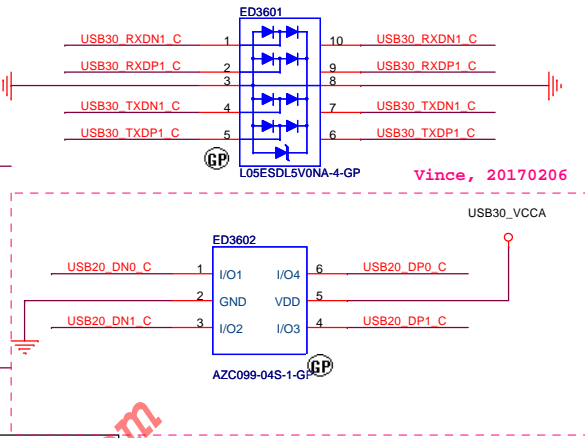
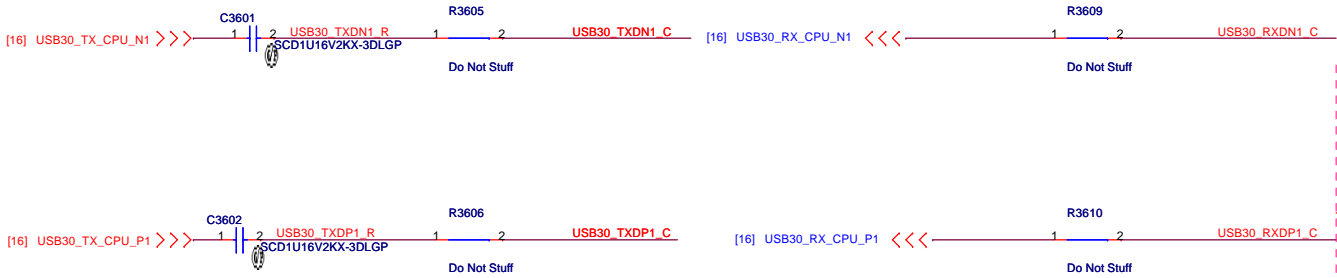
Date: Friday, June 30, 2017

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SSD = USB3.0 Port1

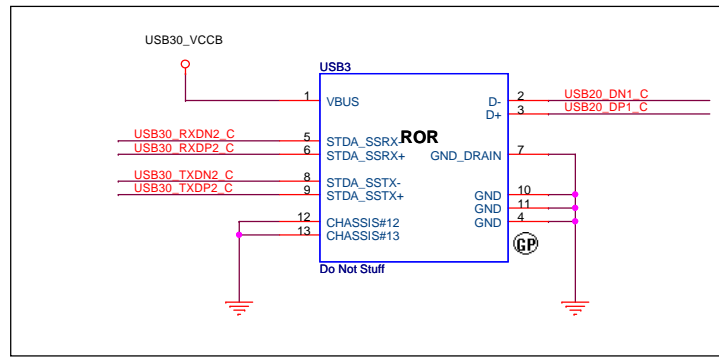
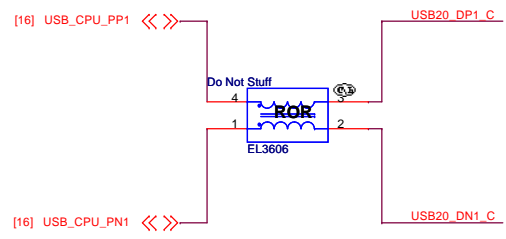
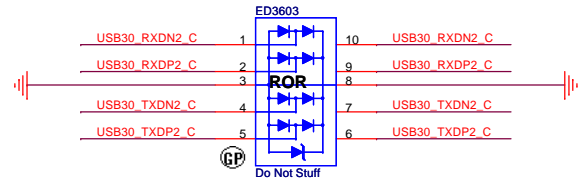
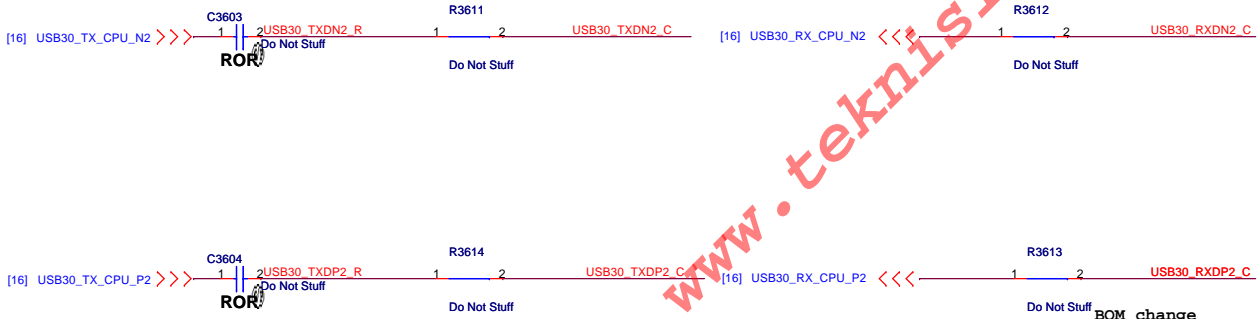
USB2.0 Port2 and USB2.0 Port3 are on IOBD

USB3.0 Port1



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

USB3.0 Port2



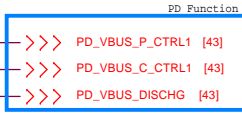
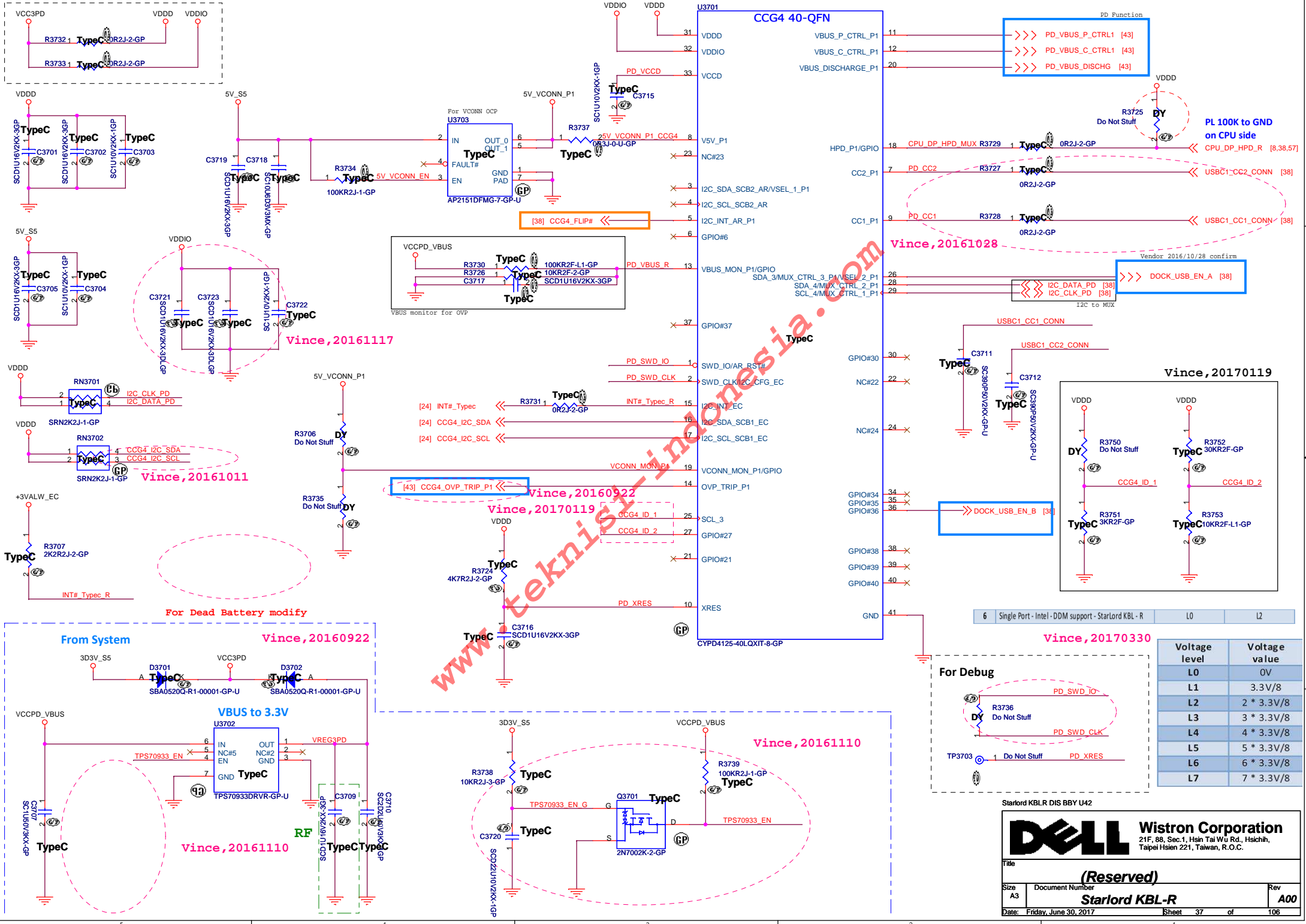
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Title: **USB30**

Size A3 Document Number: **Starlord KBL-R** Rev: **A00**

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PL 100K to GND on CPU side
CPU_DP_HPD_R [8,38,57]


Vince,20161028

Vendor 2016/10/28 confirm

Vince,20170119

Vince,20170330

Voltage level	Voltage value
L0	0V
L1	3.3V/8
L2	2 * 3.3V/8
L3	3 * 3.3V/8
L4	4 * 3.3V/8
L5	5 * 3.3V/8
L6	6 * 3.3V/8
L7	7 * 3.3V/8



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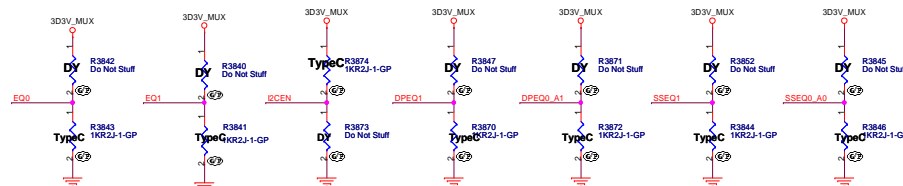
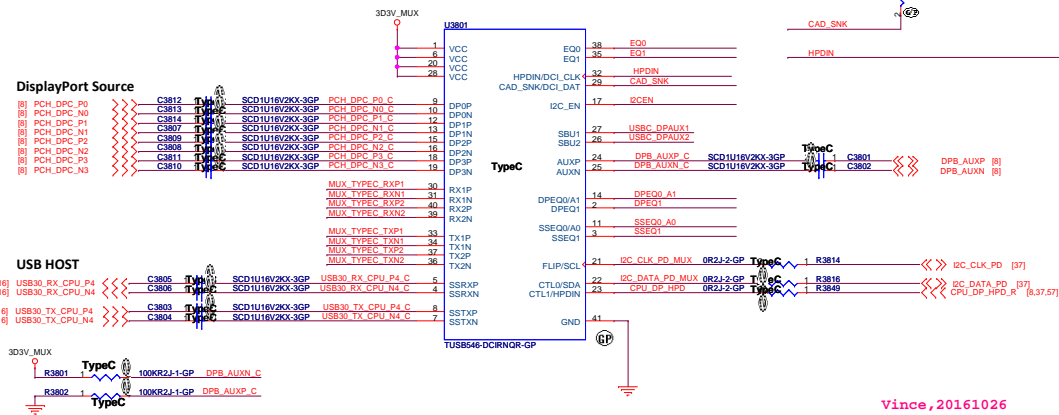
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Size: A3	Document Number: Starlord KBL-R	Rev: A00
Date: Friday, June 30, 2017	Sheet: 37	of: 106

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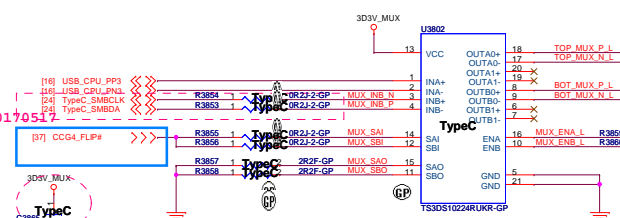
Main Func = TYPEC MUX

Vince, 20161012

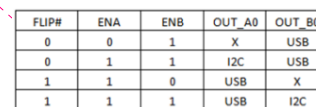
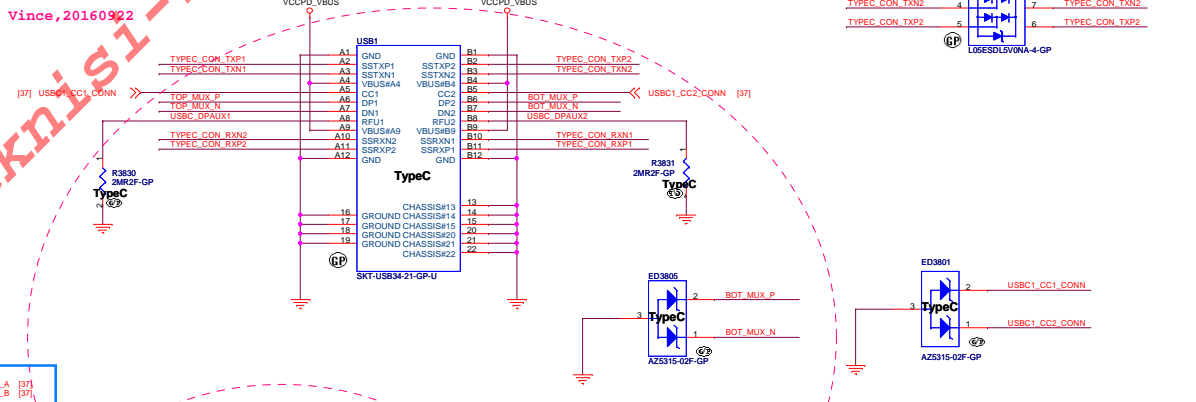
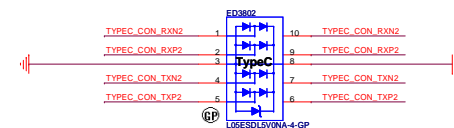
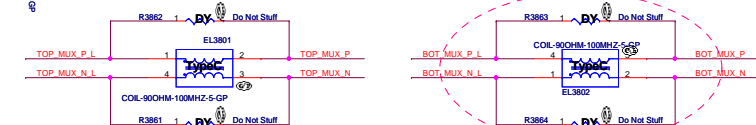


FLIP POL	CFR AMSEL	CFR1 EN	Mux Operation
X	LOW	LOW	POWER DOWN
LOW	LOW	HIGH	4-lane Orientation 1
HIGH	LOW	HIGH	4-lane Orientation 2
LOW	HIGH	HIGH	2-lane Orientation 1
HIGH	HIGH	HIGH	2-lane Orientation 2
LOW	HIGH	LOW	USB3.1 only Orientation 1
HIGH	HIGH	LOW	USB3.1 only Orientation 2

	DCI	non-DCI
23 CFLI/HFDIN	DP ENABLE in GPIO mode MPD in I2C mode	DP Enable in GPIO mode, Unused in I2C mode
29 CAD_SNK/DCI_DAT	AUX Snoop EN in GPIO mode DCI_DAT in I2C mode	AUX Snoop EN in GPIO mode EN in I2C mode
32 DCI_CLK	HPD in GPIO mode DCI_CLK in I2C mode	HPD



Vince, 20161004



FLIP#	ENA	ENB	OUT_A0	OUT_B0
0	0	1	X	USB
0	1	1	I2C	USB
1	1	0	USB	X
1	1	1	USB	I2C

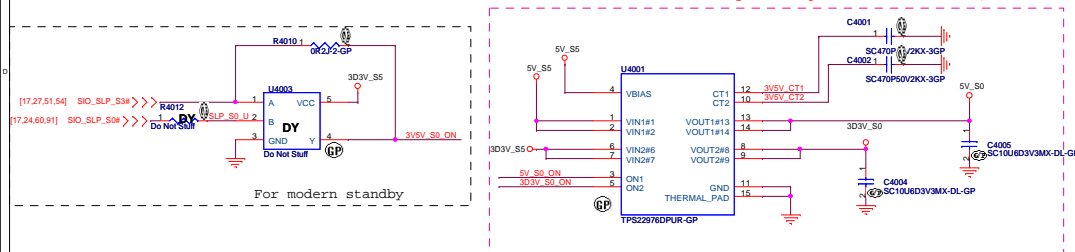


Main Func = USB3.0 Port1

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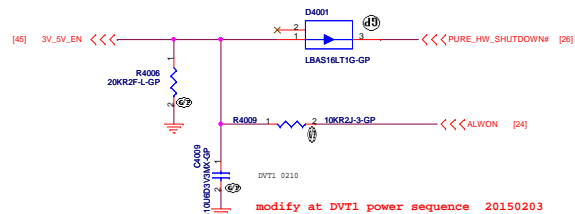
SSID = Power Plane & Sequence

ROSA Run Power



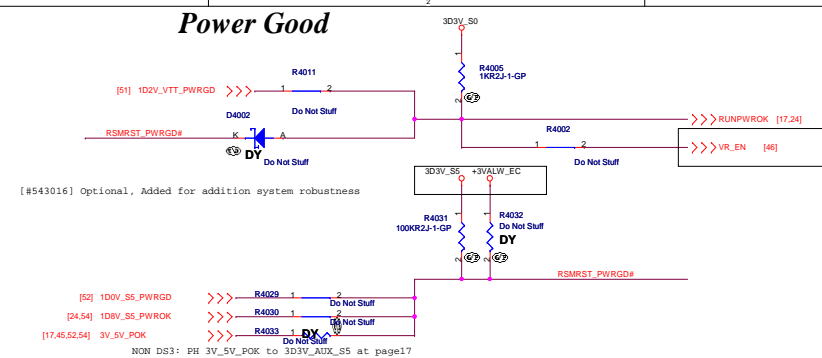
5V_S0

5V_S0 Consumption
Peak current 5A
3D3V_S0 Consumption
Peak current 2.5A

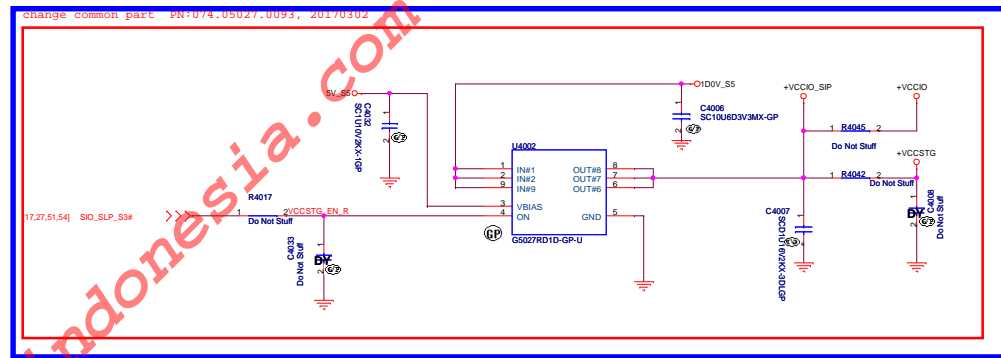


20150116 2032

Power Good



VCCIO and VCCSTG



EOPIO and EDRAM

Vince,20161027

+V_EDRAM_VR

Voltage = 1.0 V ± 50 mV
Imax = 6 A
Rds on = 4.65mohm
TRISE = 240 us

+V_EOPIO_VR

Voltage = 1.0 V ± 50 mV
Imax = 2.8 A
TRISE = 240 us

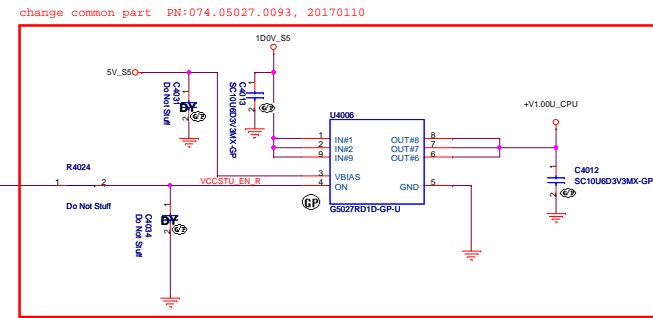
V1.8S

Vince,20161012

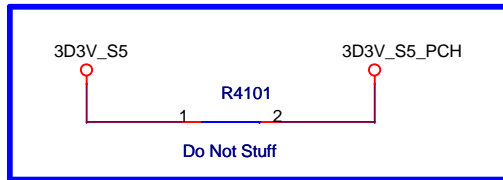
MANAGEMENT RAIL POWER GENERATION

VCCST, VCCIO, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

VCCST



Main Func = Power Plane & Sequence



Reserve by NON DS3 function 20150413

Vince,20161031

DS3

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Title

Connected_Standby(1/2)+DS3

Size
A4

Document Number

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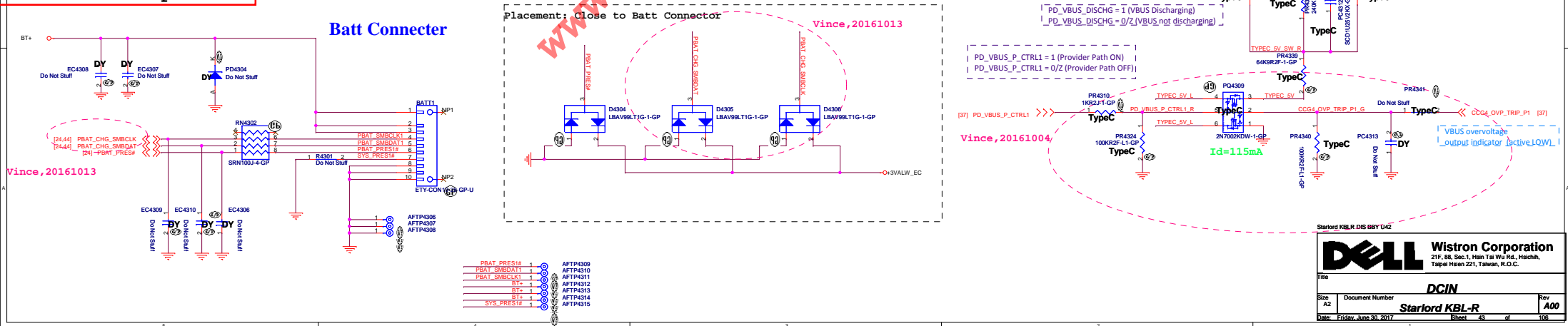
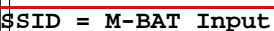
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Main Func = DIMM1
Main Func = DIMM2

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Pin Definition: TBD



Vince, 20161011

Vince, 20161013

Vince, 20160926

Vince, 20170105

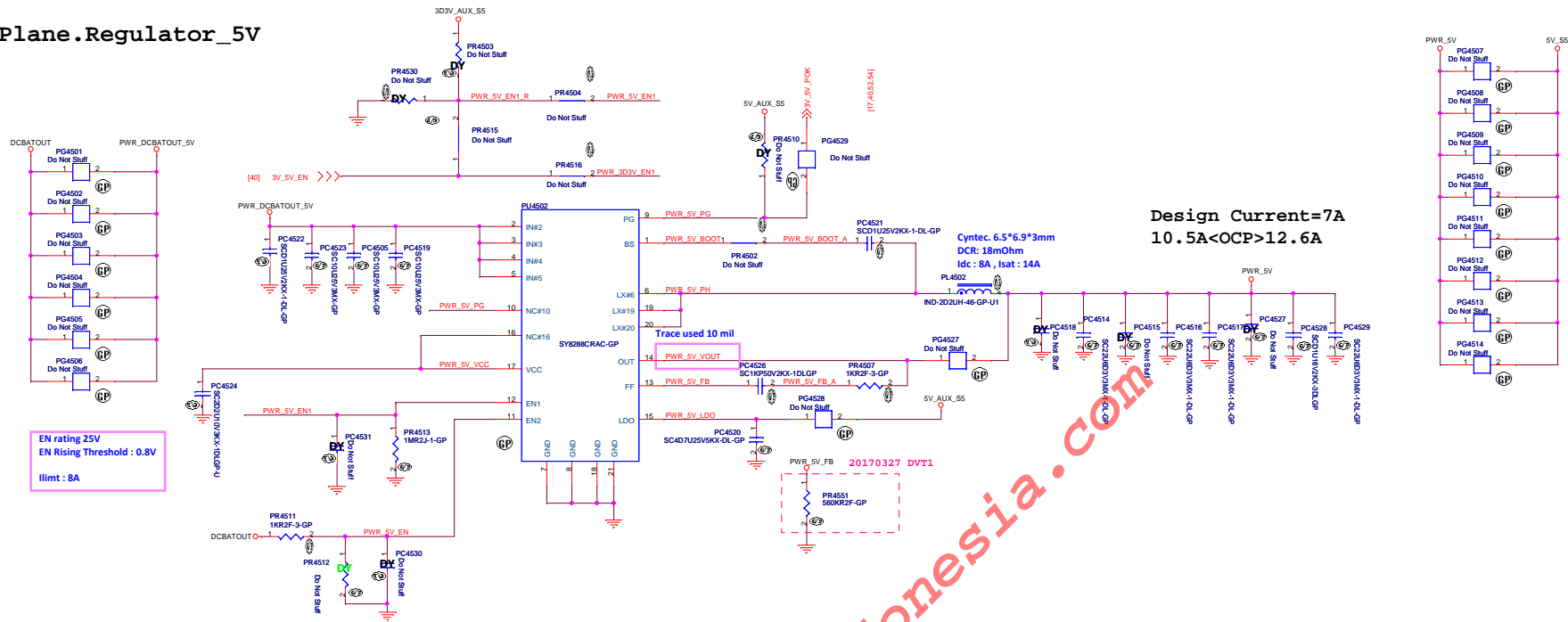
Switching frequency is 350KHz

PR4433	2 cell	3 cell	4 cell
INVC	100k	66.5k	62.5k
HYBRID	165k	182k	147k

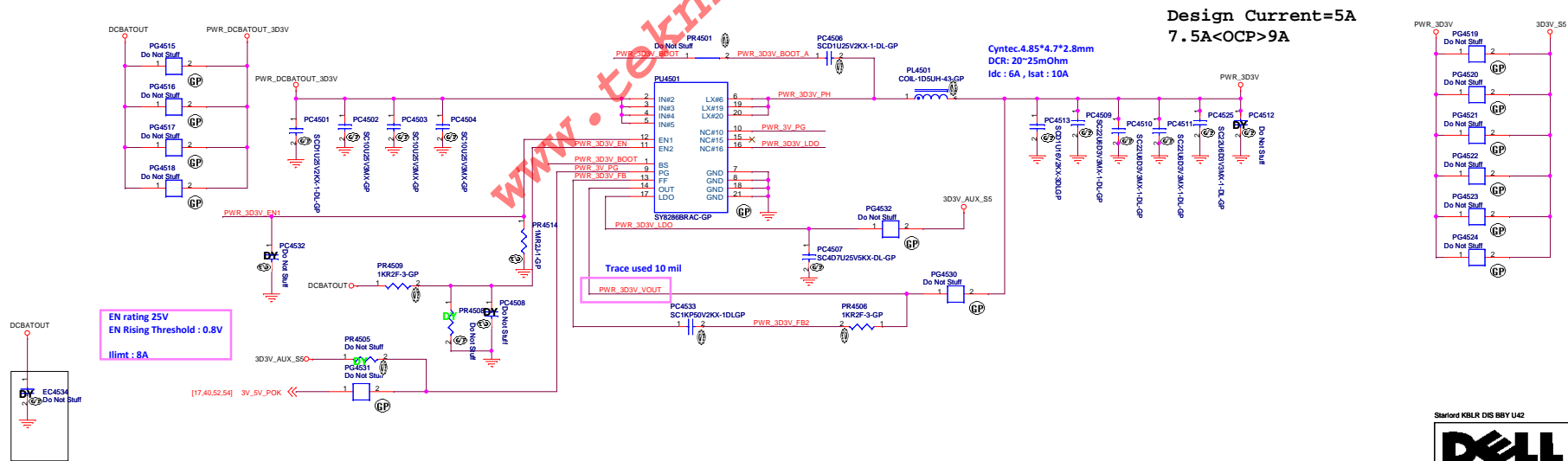
RP request 2016/01/12 modify

CHECK EE follow customer circuits.

SSID = PWR.Plane.Regulator_5V



SSID = PWR.Plane.Regulator_3D3V




20170208

Main Func = CPU_CORE

(Blanking)

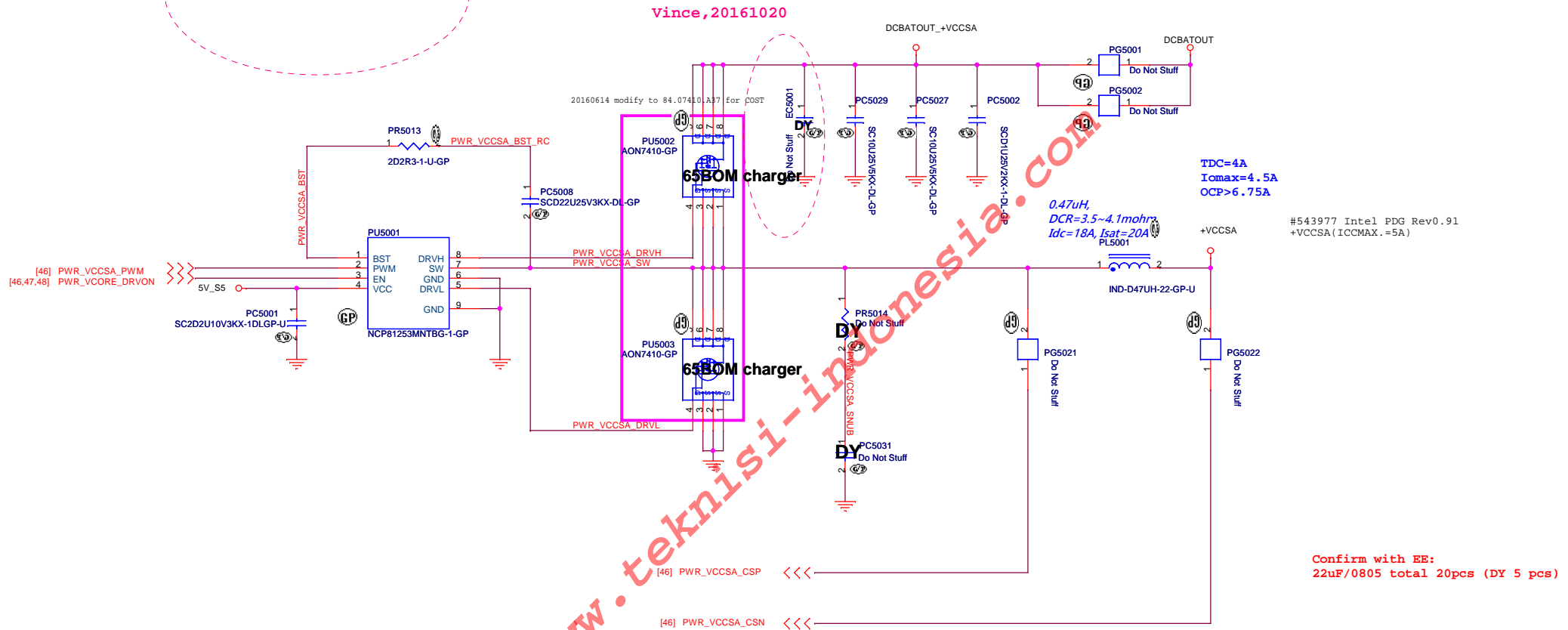
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Title		NCP81210MN_CPU_VCCGTUS	
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Main Func = CPU_CORE

Vince,20160922



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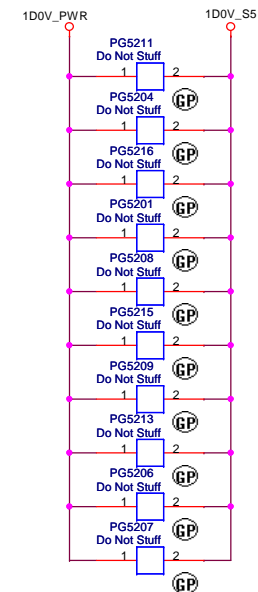
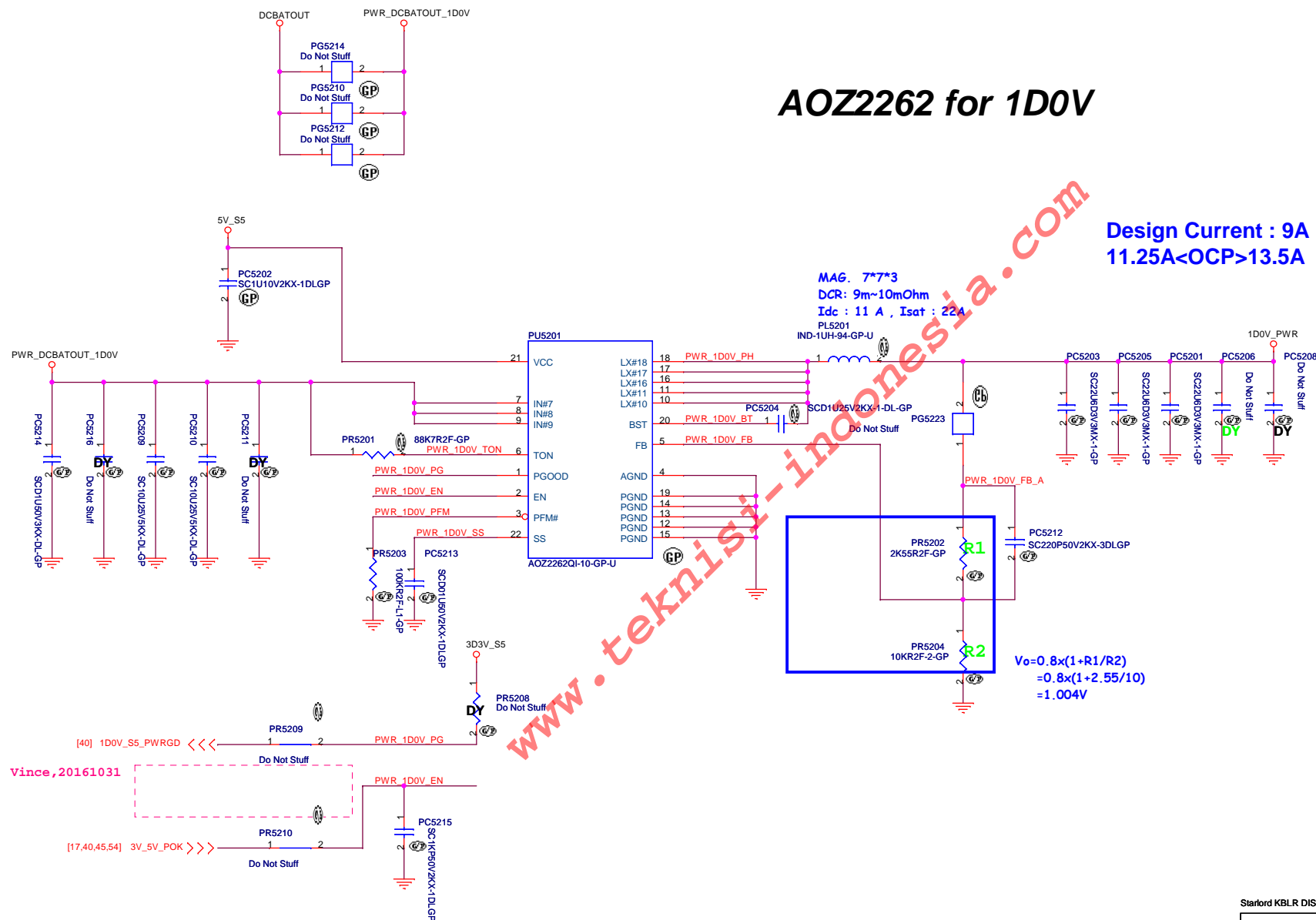
Wistron Corporation
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Title			NCP81253MN_CPU_VCCSA	
Size	Document Number	Starlord KBL-R		Rev
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```
SSID = PWR.Plane.Regulator_1D0V
```

AOZ2262 for 1D0V

Design Current : 9A
11.25A<OCP>13.5A



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Title			
(Reserved)			
Size A3	Document Number	Rev	
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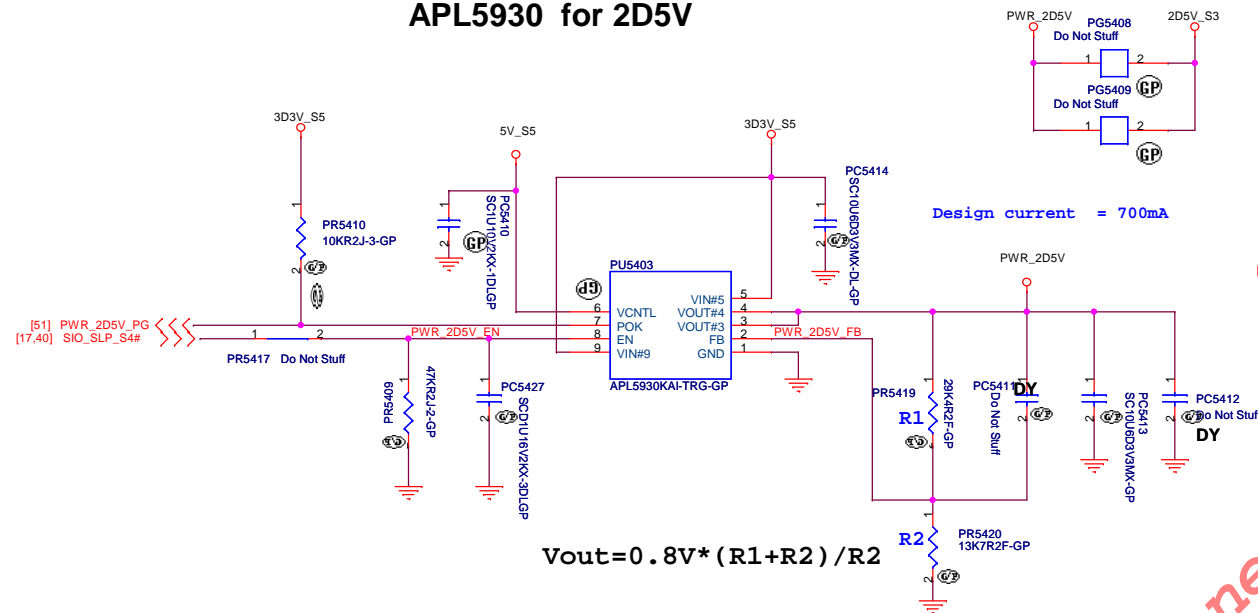
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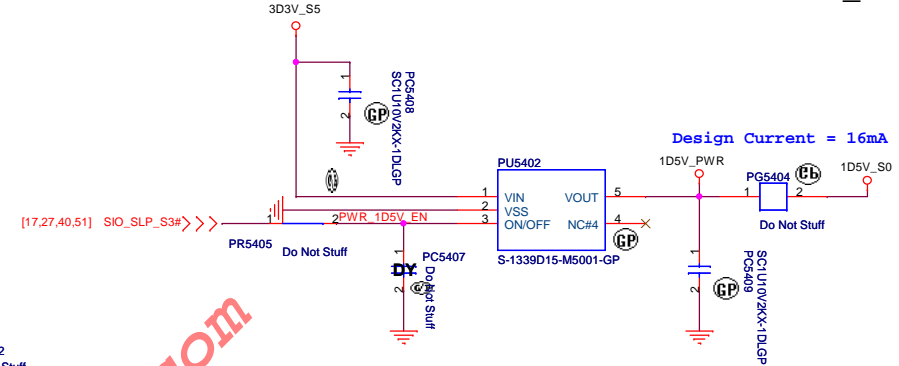
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
(Reserved)			
Size	Document Number		Rev
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SSID = 1D5V

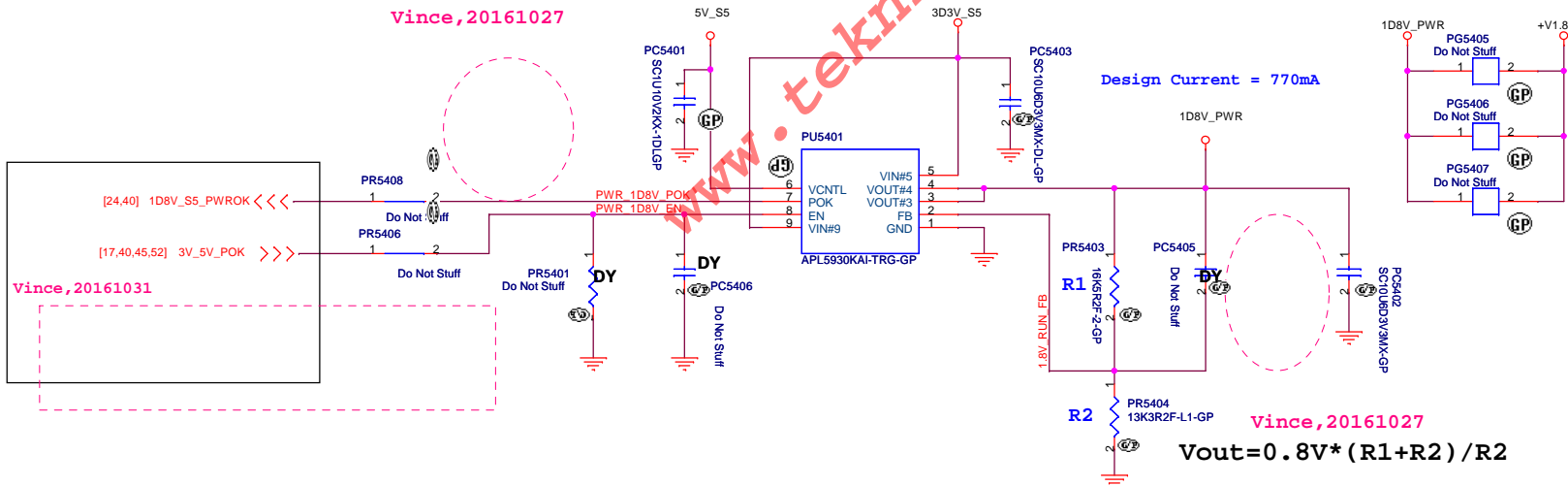
APL5930 for 2D5V

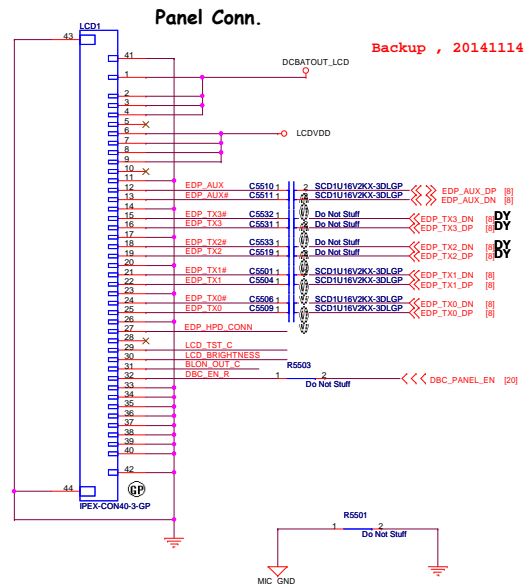


S-1339D15-M5001 for 1D5V_S0



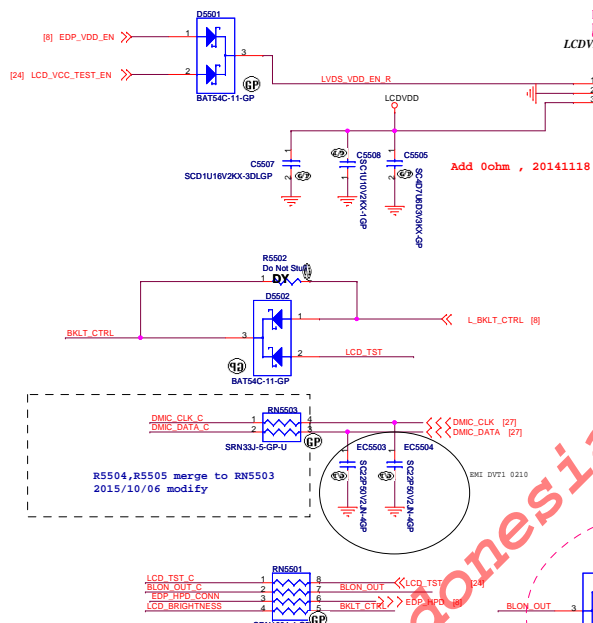
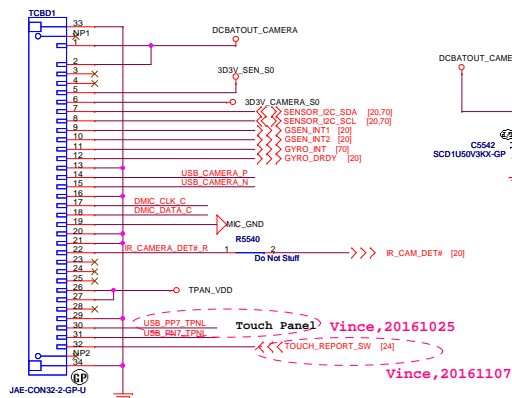
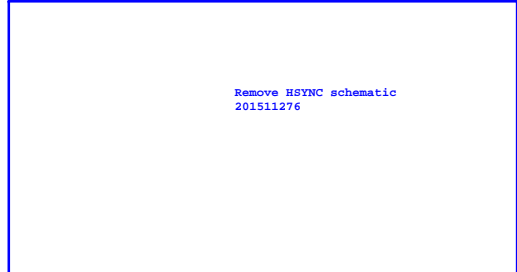
APL5930 for 1D8V_S5



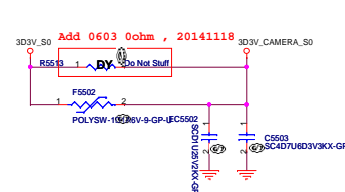


Power Pin Count : 7
GND Pin Count : 9

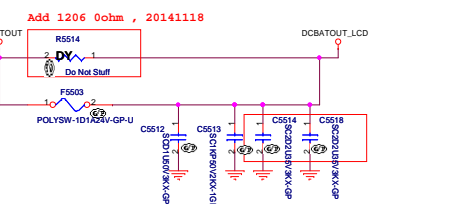
HSYNC



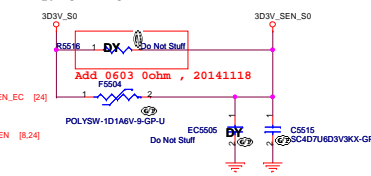
CAMERA POWER



INVERTER POWER

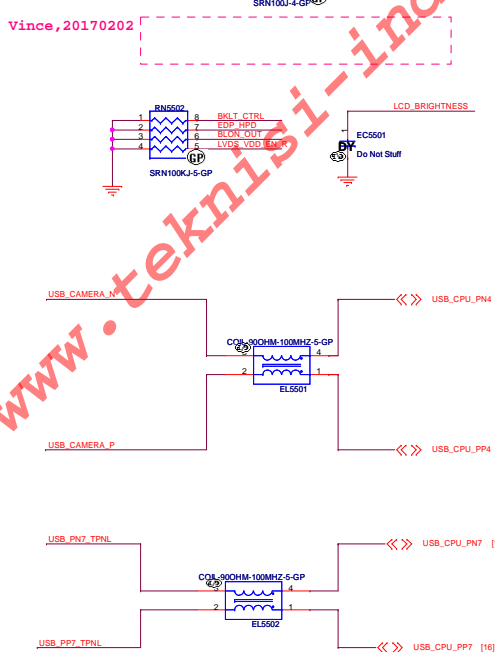
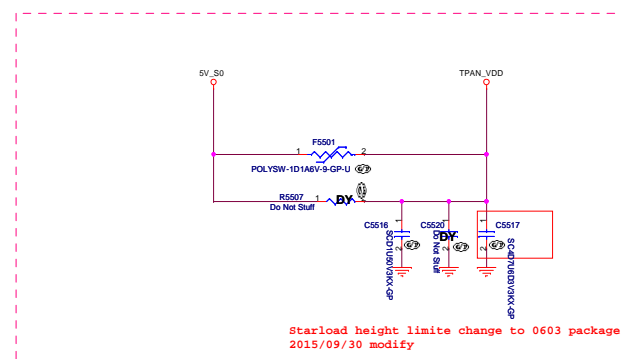


SENSOR POWER




TOUCH PANEL POWER

Vince, 20161202

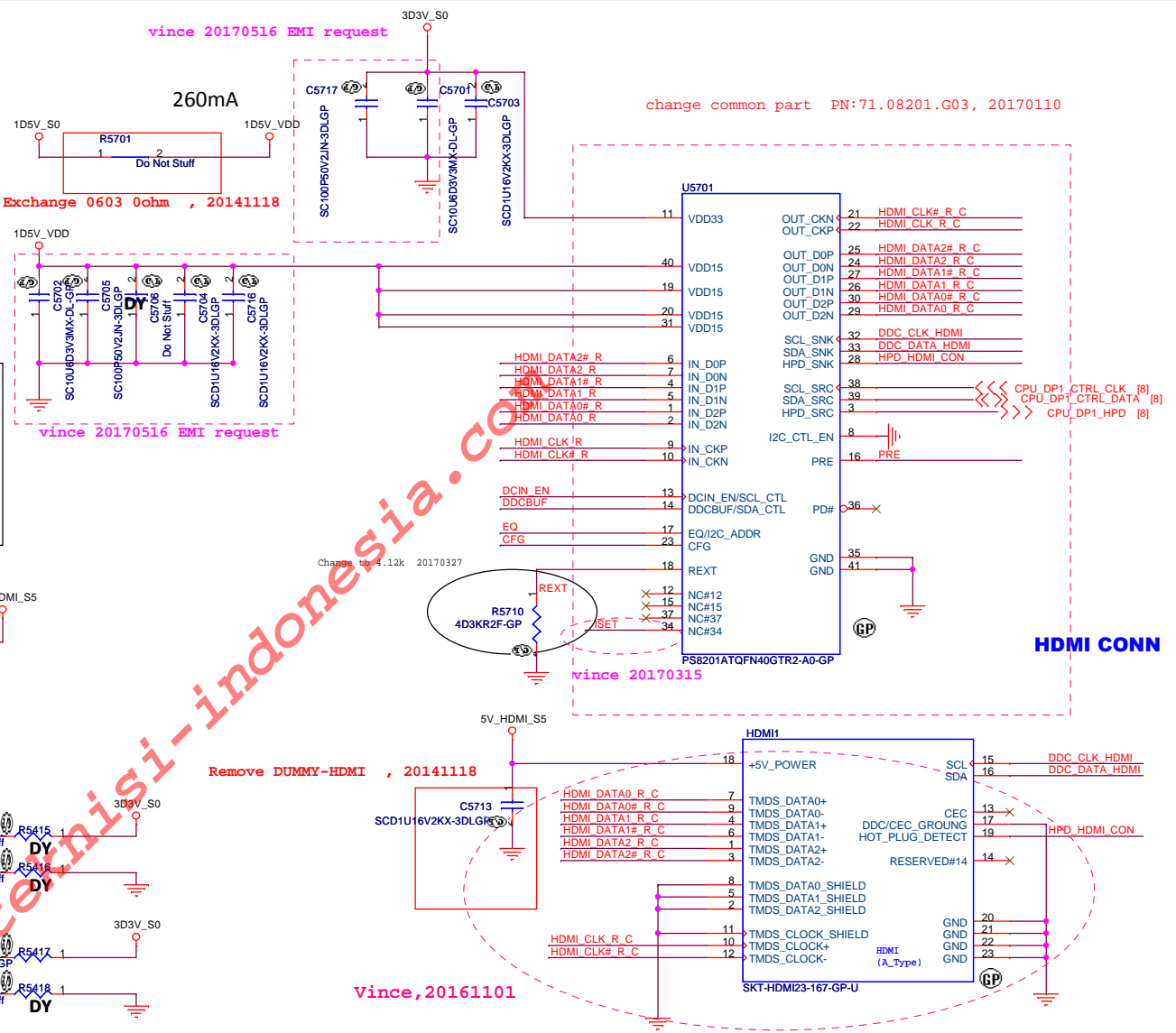
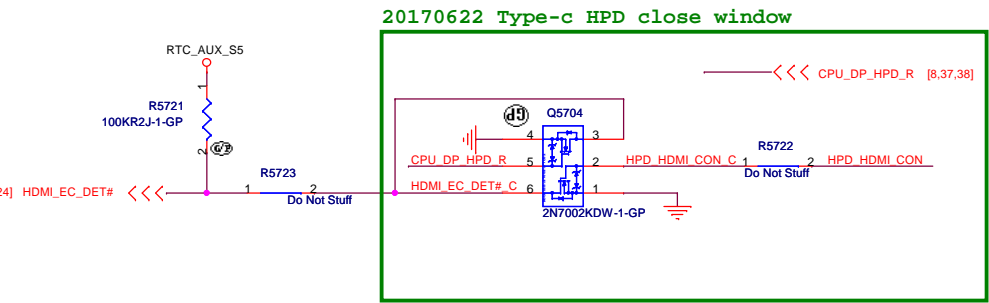
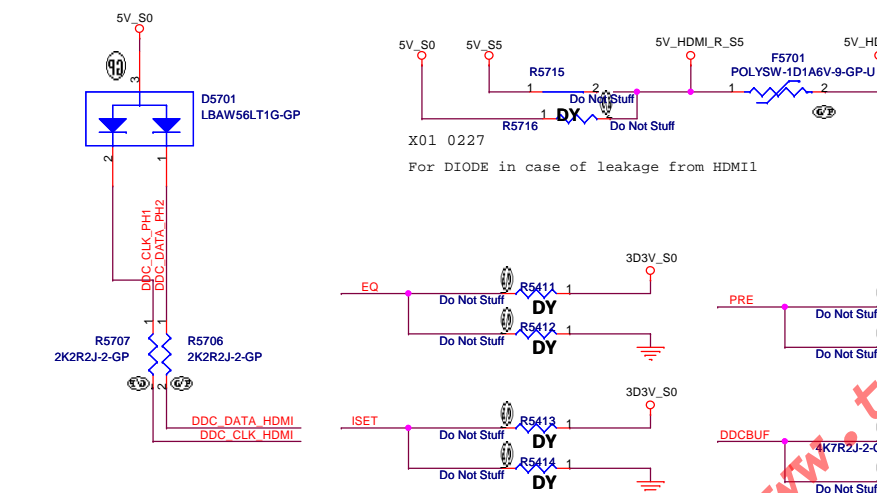
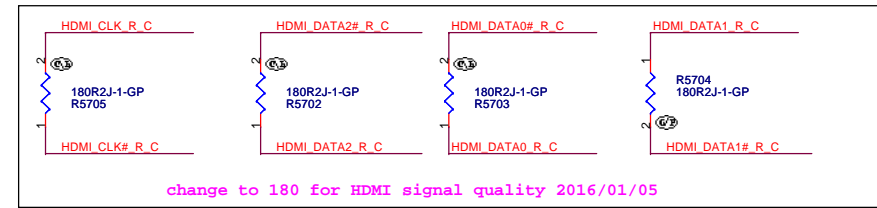


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Title CRT		
Size A2	Document Number Starlord KBL-R	Rev A00
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SSID = HDMI



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Title			(Reserved)	
Size	Document Number	Rev		
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Main Func = WLAN

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Title			
NGFF WLAN CONN			
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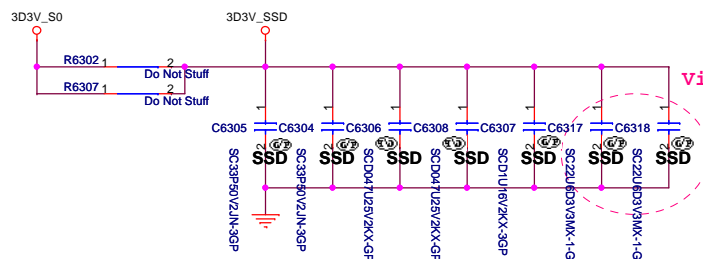
Rev
A00

Date: Friday, June 30, 2017

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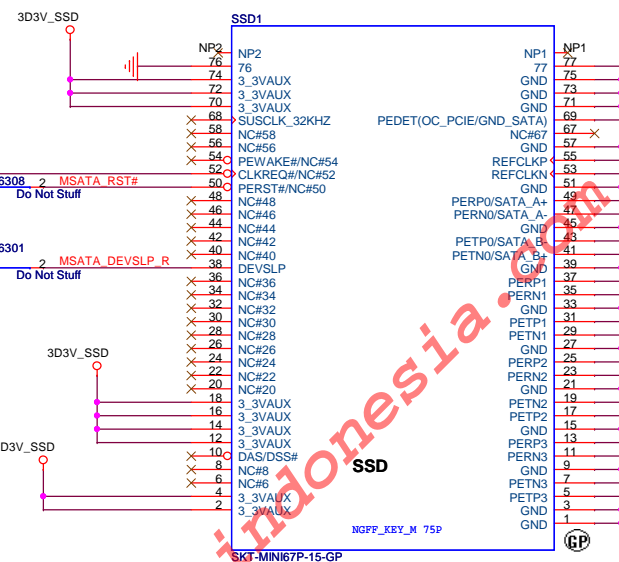
SSD = M.2

Vince,20160929

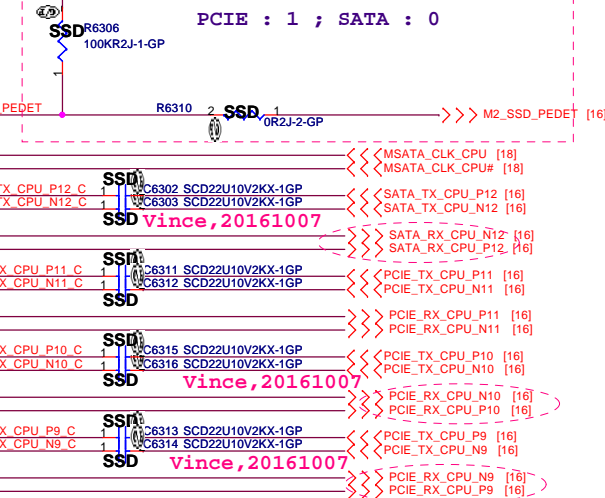


Vince,20161028

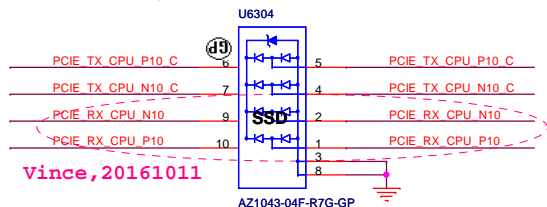
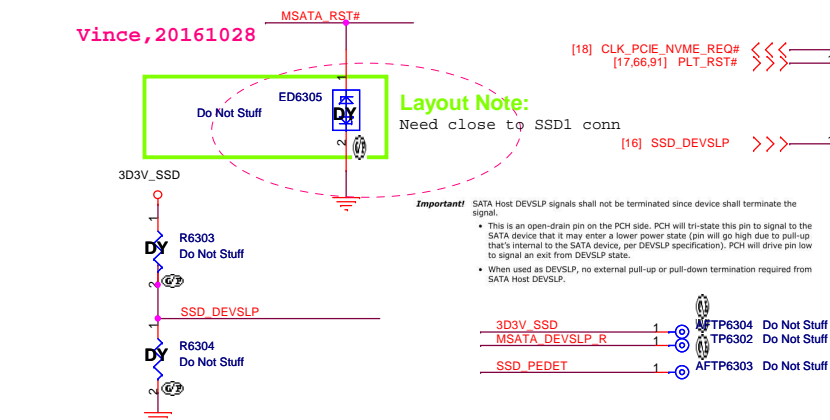
SSD M.2 CONN



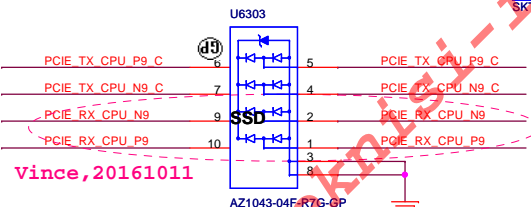
Vince,20161103



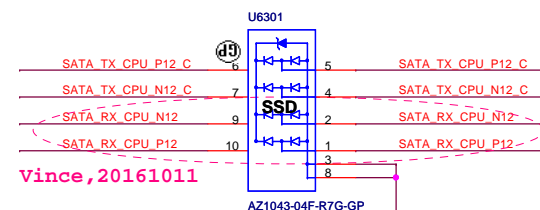
Vince,20161028



Vince,20161011



Vince,20161011



Vince,20161011

Table 13-12. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2 / SATA	PCI Express* Gen 3 / SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

Notes:

- Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe* Gen 2 / SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe* Gen 3 / SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.
- Design Constraint: For PCIe* lane that needs to support either PCIe* Gen2 devices or PCIe* Gen3 devices, follow the PCIe* Gen 3 / SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

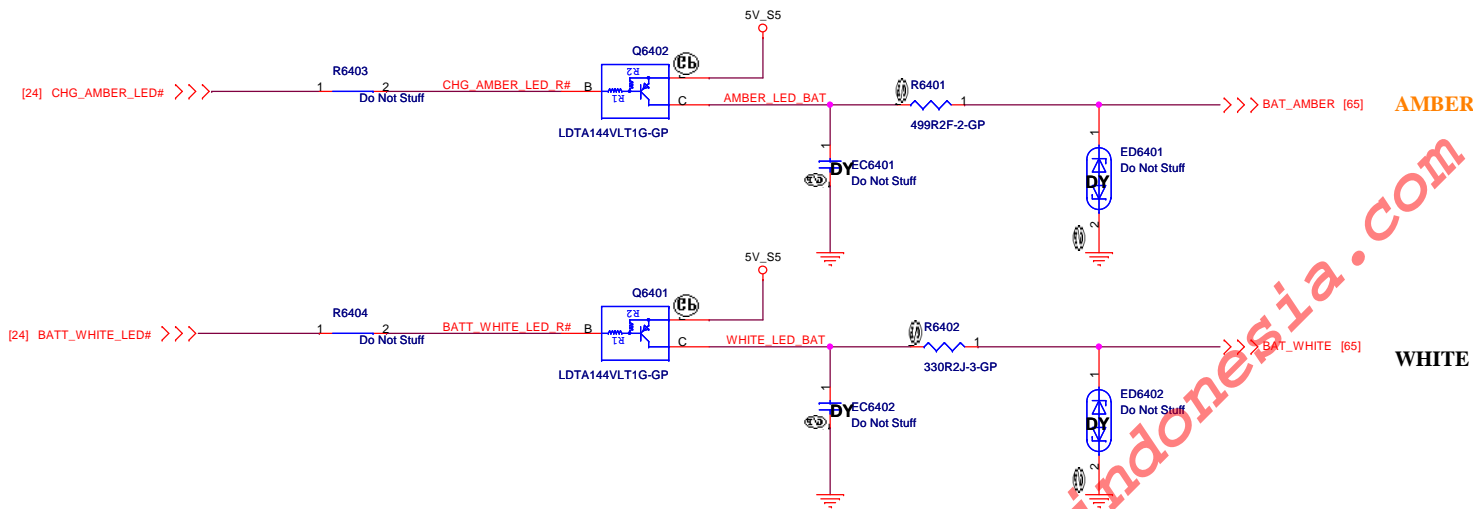
74	SSD	75	SSD
72	SSD	73	SSD
70	SSD	69	SSD
68	SSD	67	SSD
66	SSD	65	SSD
64	SSD	63	SSD
62	SSD	61	SSD
60	SSD	59	SSD
58	SSD	57	SSD
56	SSD	55	SSD
54	SSD	53	SSD
52	SSD	51	SSD
50	SSD	49	SSD
48	SSD	47	SSD
46	SSD	45	SSD
44	SSD	43	SSD
42	SSD	41	SSD
40	SSD	39	SSD
38	SSD	37	SSD
36	SSD	35	SSD
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32	SSD	31	SSD
30	SSD	29	SSD
28	SSD	27	SSD
26	SSD	25	SSD
24	SSD	23	SSD
22	SSD	21	SSD
20	SSD	19	SSD
18	SSD	17	SSD
16	SSD	15	SSD
14	SSD	13	SSD
12	SSD	11	SSD
10	SSD	9	SSD
8	SSD	7	SSD
6	SSD	5	SSD
4	SSD	3	SSD
2	SSD	1	SSD

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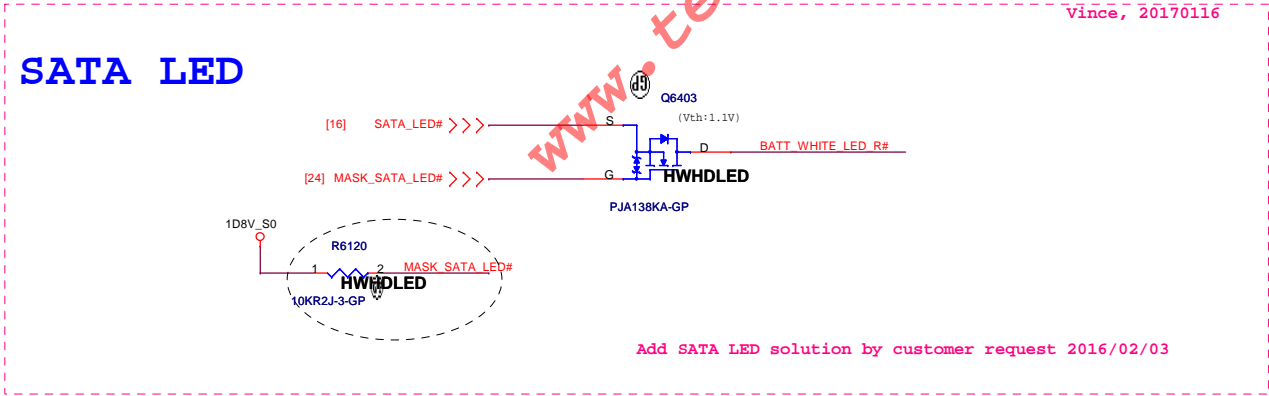
DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

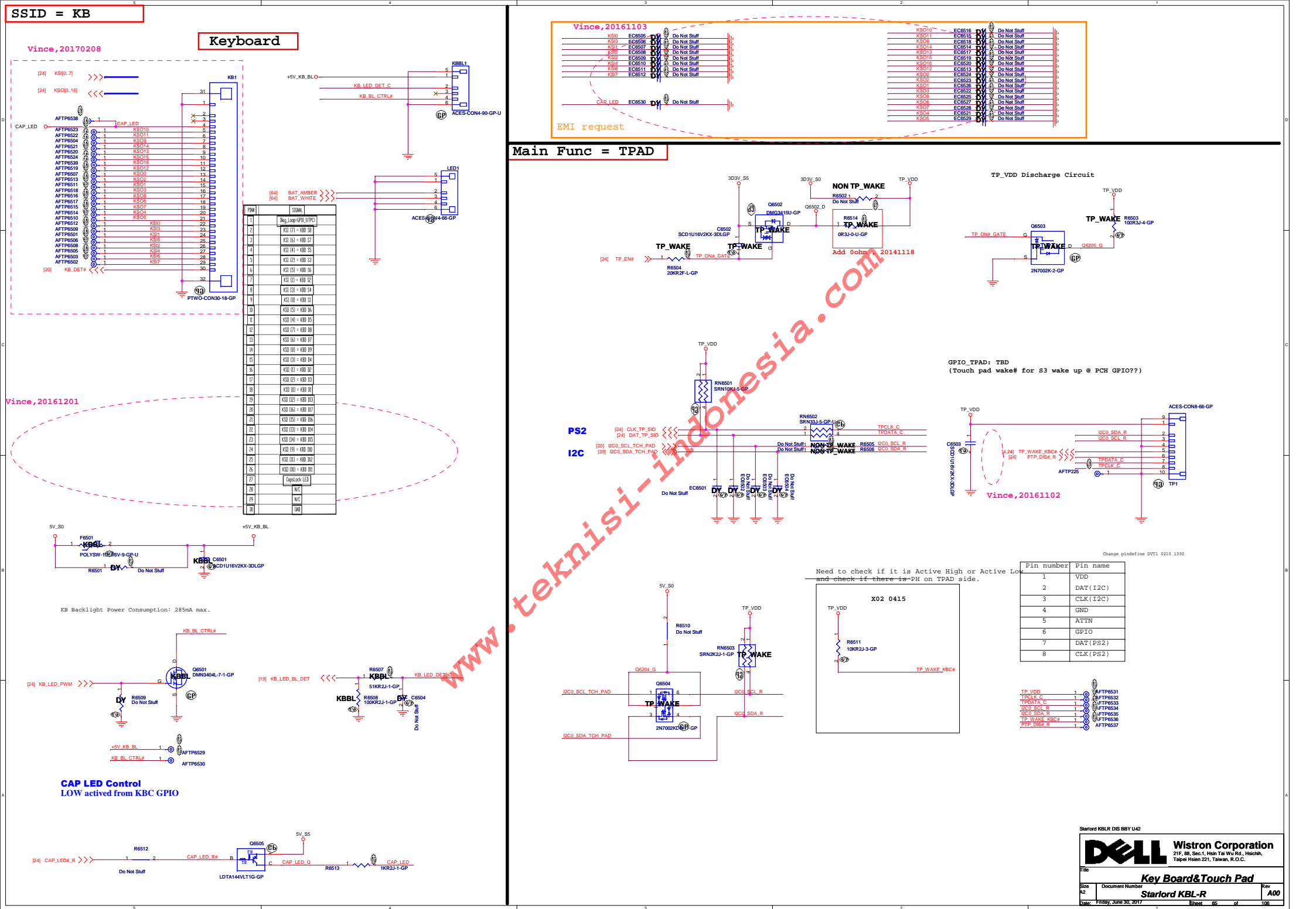
Title (Reserved)		
Size A3	Document Number	Rev A00
Starlord KBL-R		
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Battery LED1 (AMBER_LED)
Low activated from KBC GPIO

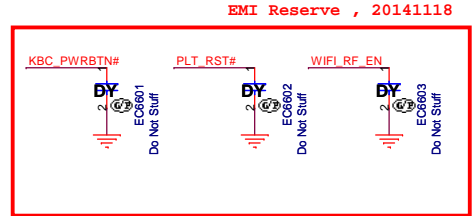
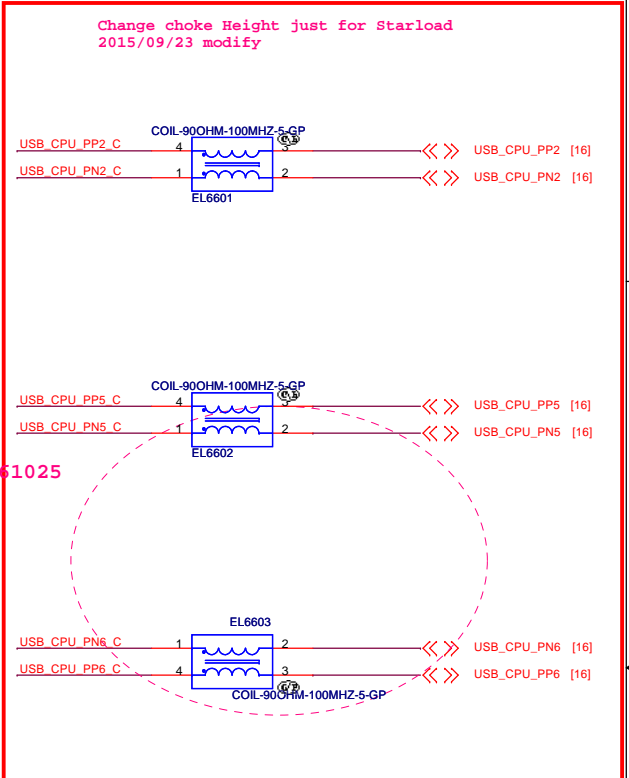
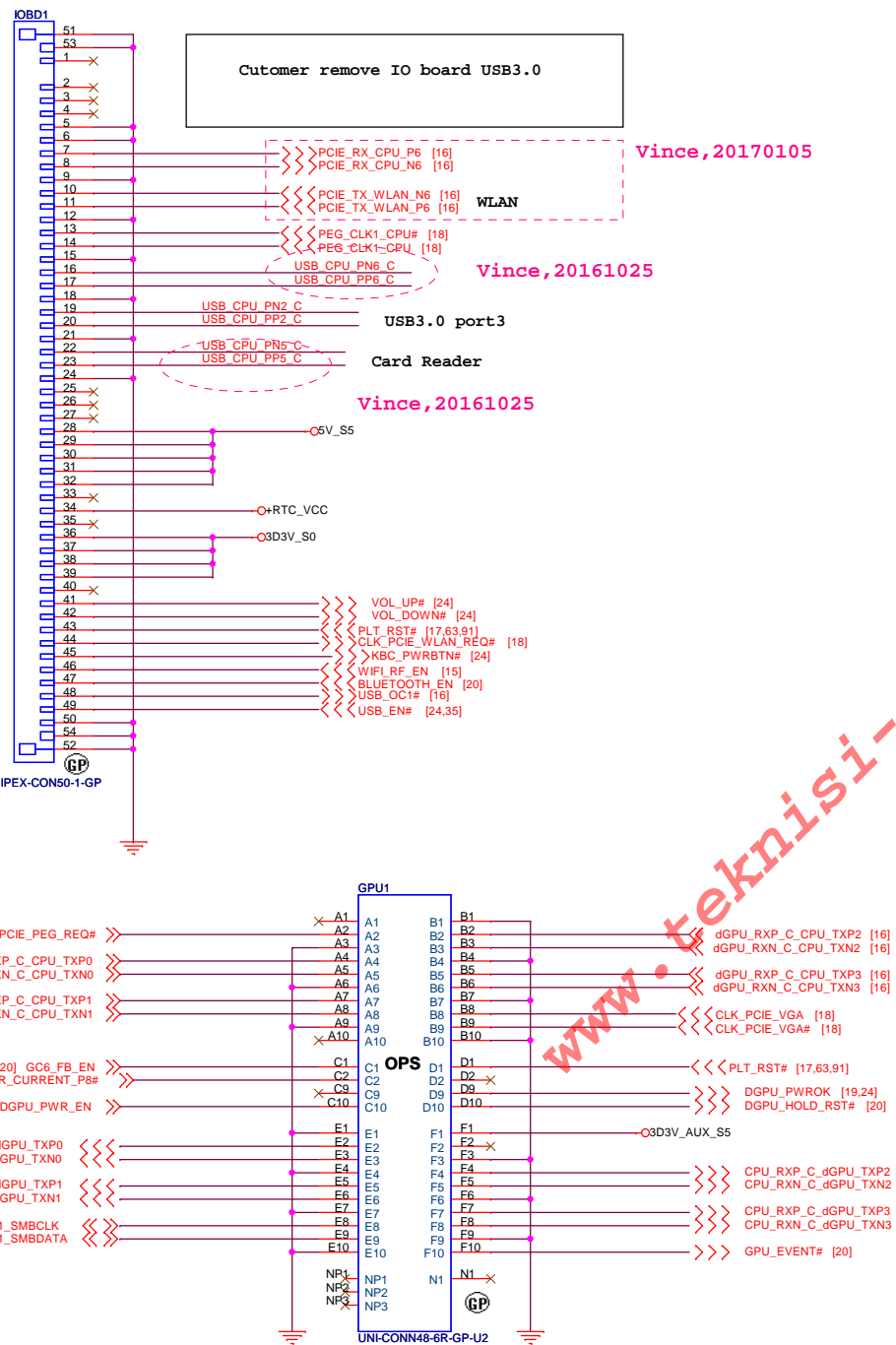


Battery LED2 (WHITE_LED)
Low activated from KBC GPIO





SSID = IO Connector



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Title

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Size
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Document Number

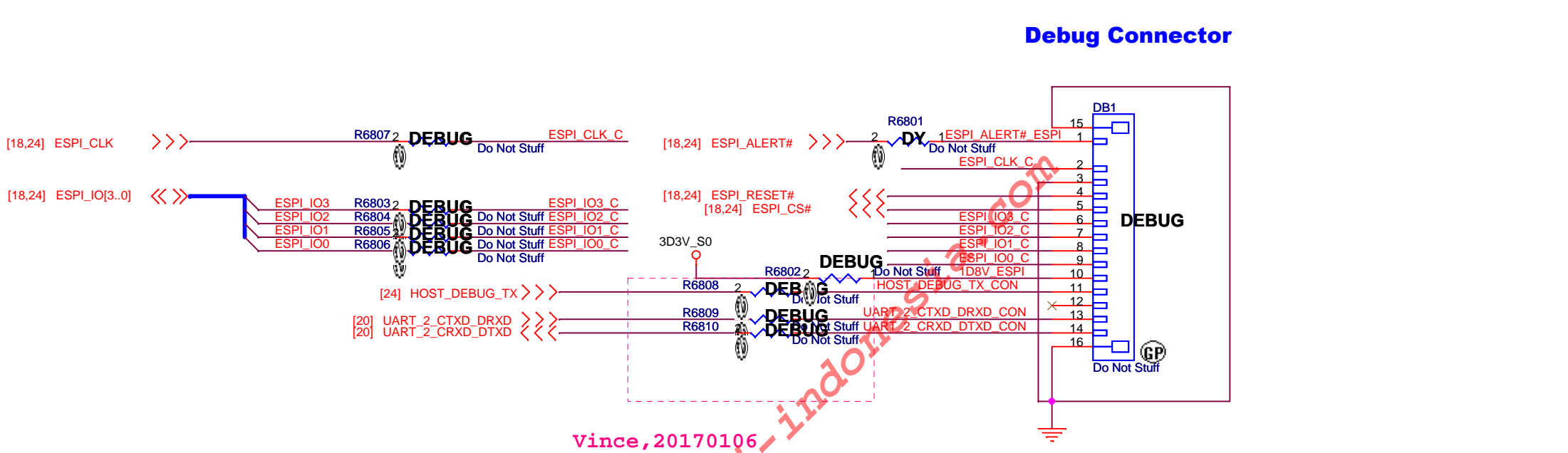
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SSID = Debug




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Title			
Dubug connector			
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Reserved

[illegible]

The second timing diagram illustrates the interaction between the Gyro, INT2, and FFS modules. It shows the following signals and their timing:

- GYRO_INT_P11**: A red signal line.
- INT2_SELECT**: A red signal line.
- FFS_INT2**: A red signal line, labeled with a red [20] at the end.
- D7001**: A blue block labeled "Do Not Stuff" with a "1" on its input and a "2" on its output.
- DY**: A blue block labeled "Do Not Stuff" with a "2" on its input and a "3" on its output.
- R7008**: A blue block labeled "Do Not Stuff" with a "1" on its input and a "2" on its output.
- FFS**: A red block labeled "Do Not Stuff" with a "1" on its input and a "2" on its output.

The diagram shows the following sequence of events:

- GYRO_INT_P11** transitions from low to high.
- INT2_SELECT** transitions from low to high.
- FFS** transitions from low to high.
- FFS_INT2** transitions from low to high.
- INT2_SELECT** transitions from high to low.
- GYRO_INT_P11** transitions from high to low.

[illegible]

- | - no via, trace, under the sensor (keep out area around 2mm)
- | - stay away from the screw hole or metal shield soldering joints
- | - design PCB pad based on our sensor LGA pad size (add 0.1mm)
- | - solder stencil opening to 90% of the PCB pad size
- | - mount the sensor near the center of mass of the NB as possible as you can

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

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GPU(55)PWR/GND

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GPU-VRAM7,8 (4/4)

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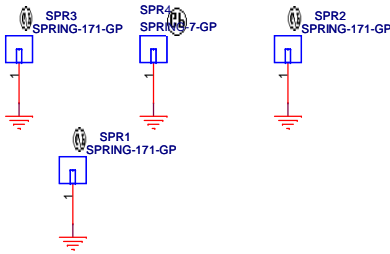
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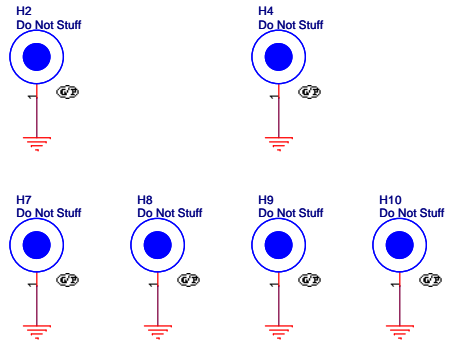
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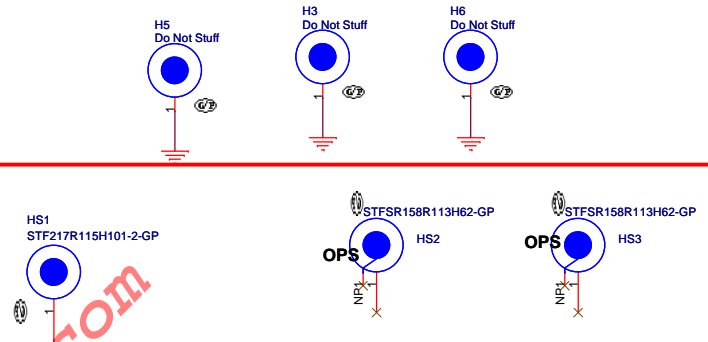


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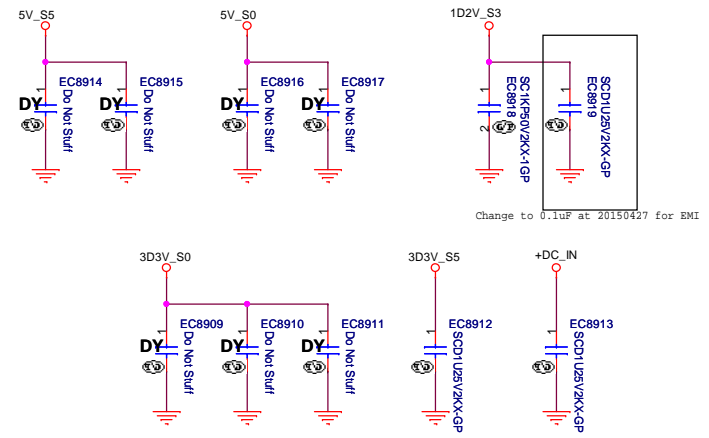
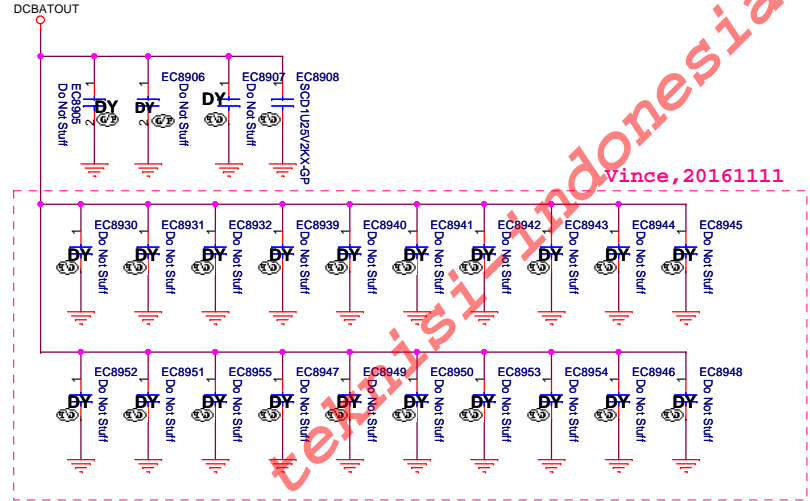
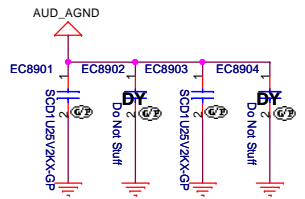
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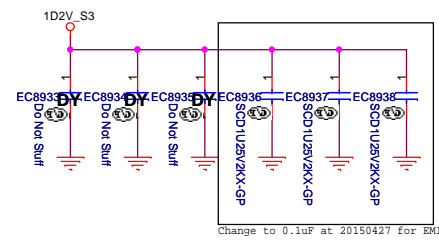
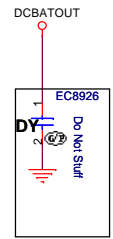
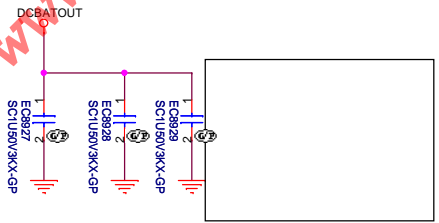
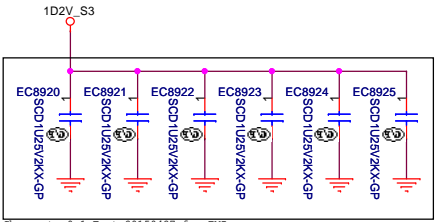
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Mind the voltage rating of the caps.



SSID = RF



Remove EC8931, EC8932, EC8926, EC8930 for placement

RF request 2016/01/12 modify

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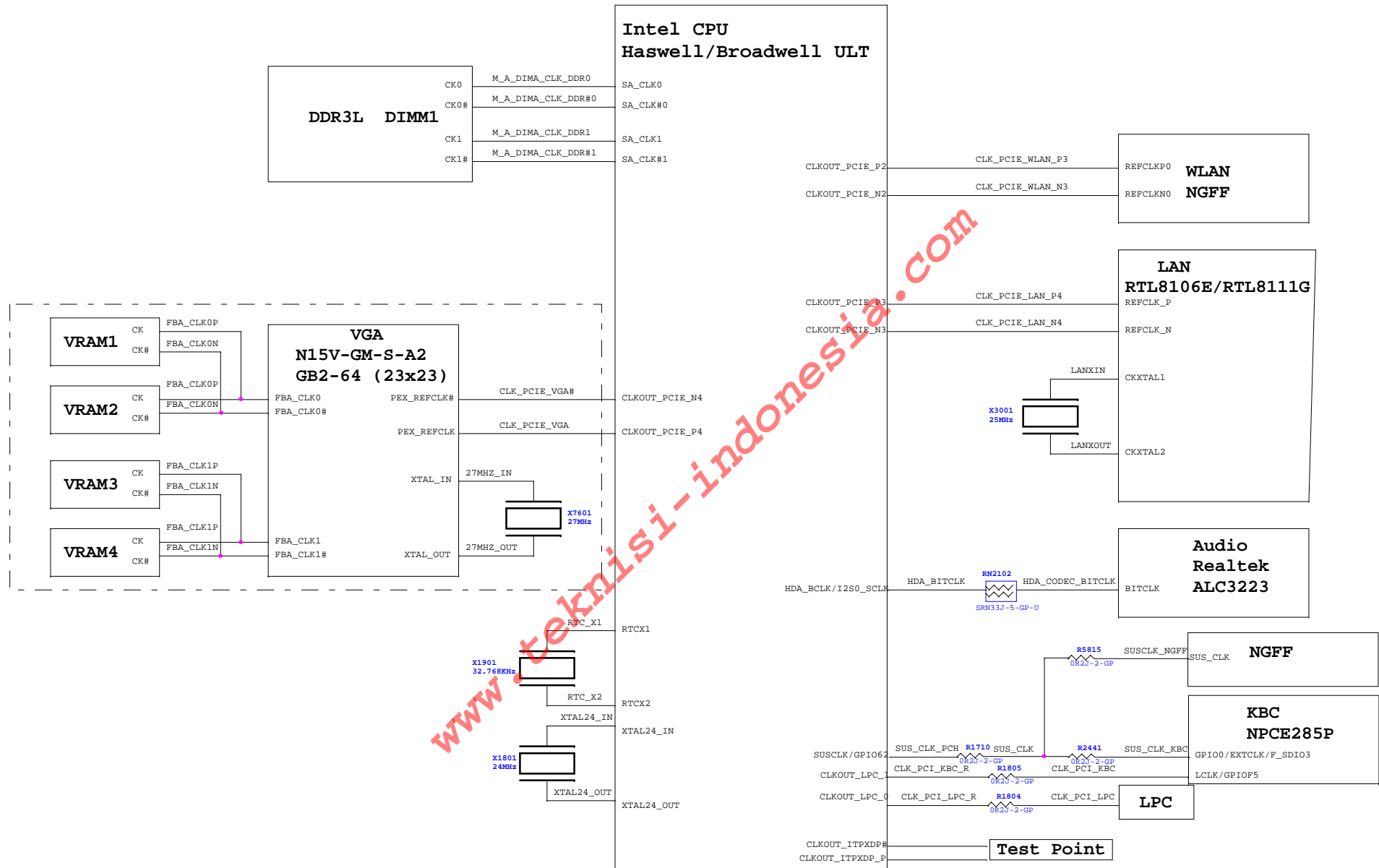
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CLK Block Diagram



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Change History

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[illegible]

The timing diagram shows three digital signals over time. The signals are 2DSV_S3, 1D2V_S3, and 0D6V_S0. 2DSV_S3 is a square wave that transitions from low to high at a certain point. 1D2V_S3 is a square wave that transitions from low to high at a later point. 0D6V_S0 is a square wave that transitions from low to high at the latest point.

Timing diagram for the PEX_VDD 1.05V supply. The diagram shows the relationship between the PEX_VDD 1.05V supply and other signals: All 3.3V, NVVDD, and FBVDDIQ. The PEX_VDD 1.05V signal is shown as a step function that rises after the 3.3V signals and before the NVVDD signal. The timing is defined by 90% and 10% thresholds.

Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

The following timing diagram in Figure 18-12 and Table 18-3 describes the GC6 2.0 en and exit sequence and timing requirements.

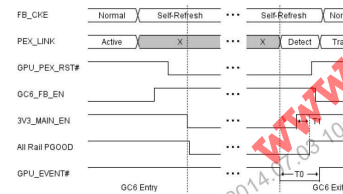


Figure 18-12. GC6 2.0 Entry/Exit Sequence Timing Diagram

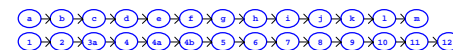
Table 18-2. GC6 2.0 Entry/Exit Sequence Timing Parameters

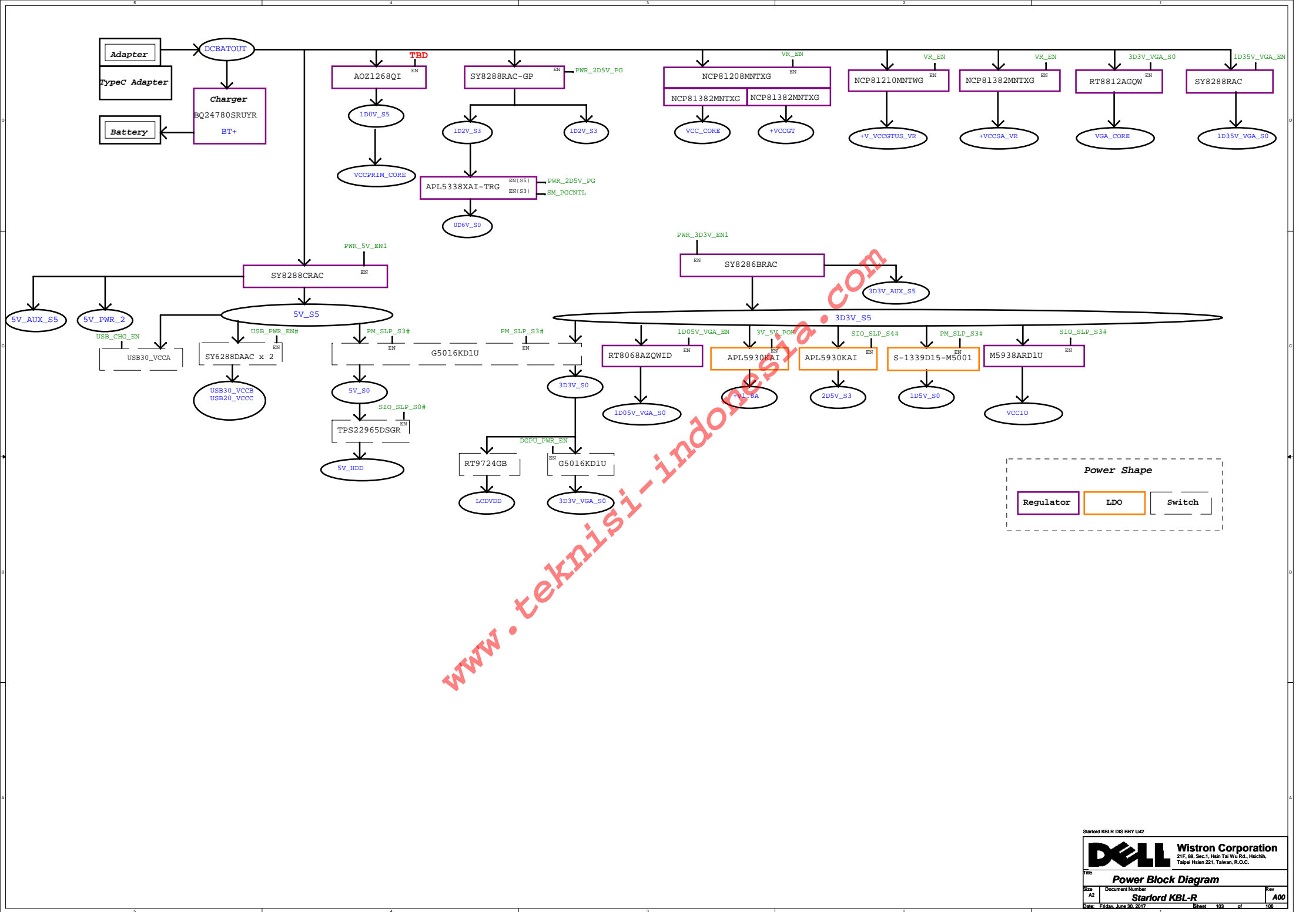
Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

There is no specific power down sequence. However, residual voltage from power down must not violate the power-up sequence when back to back GPU power-down and power-up events take place.

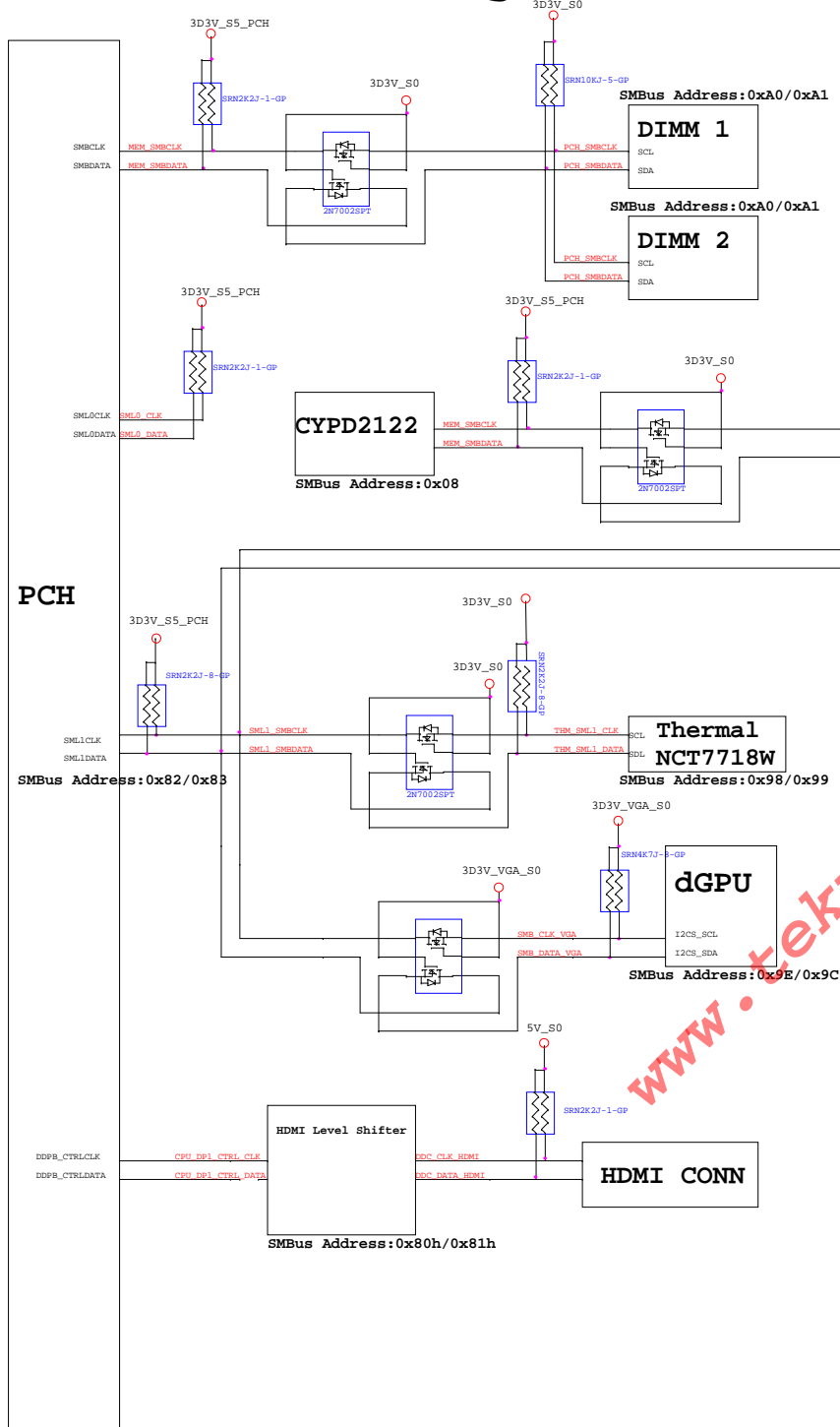
Note:

- All RAIL PG00DN1 presents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
- During GC6 exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/O stays on.
- All delays should be minimized to increase time spent in GC6 for maximum power saving.
- The entire entry/exit sequence must complete within 200 ms.

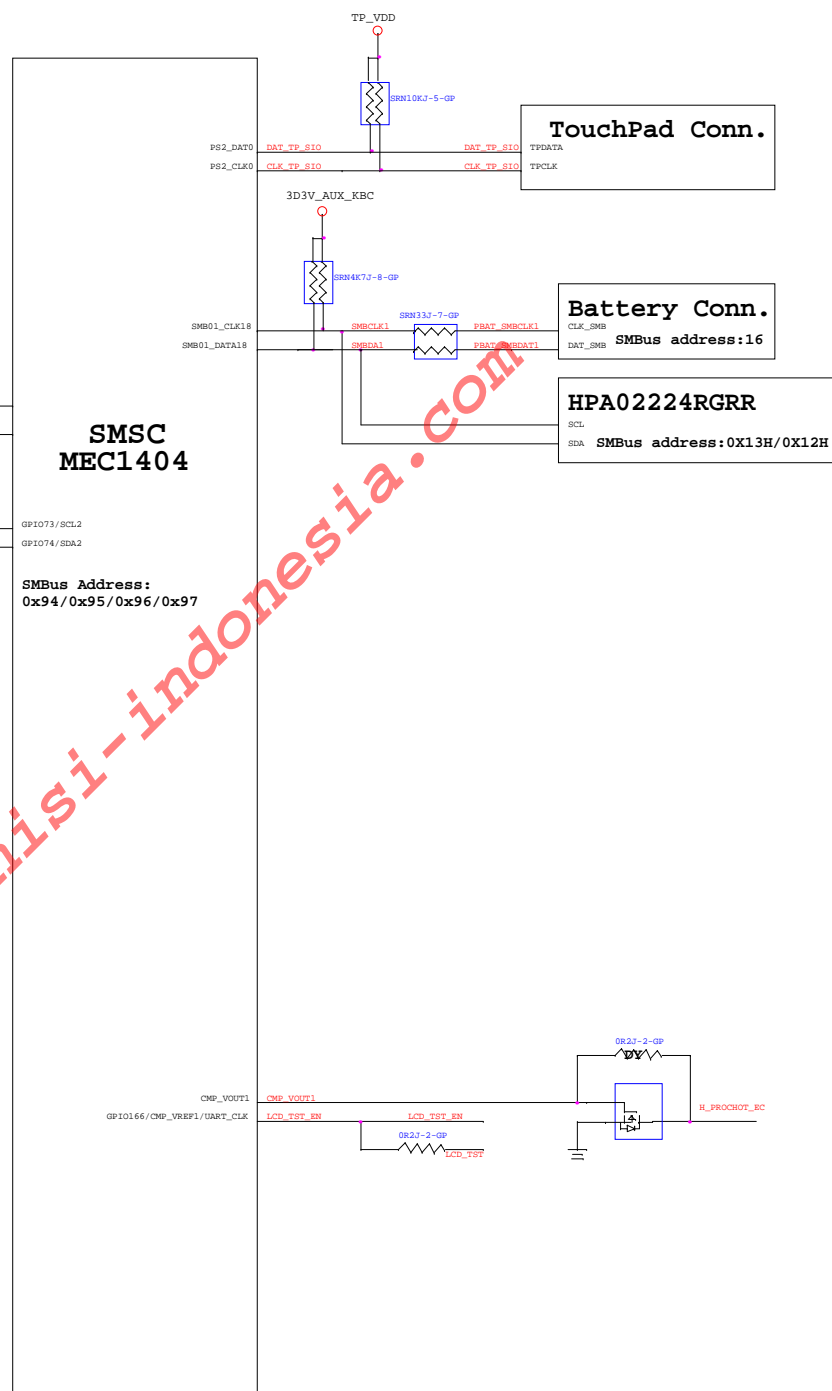




PCH SMBus Block Diagram

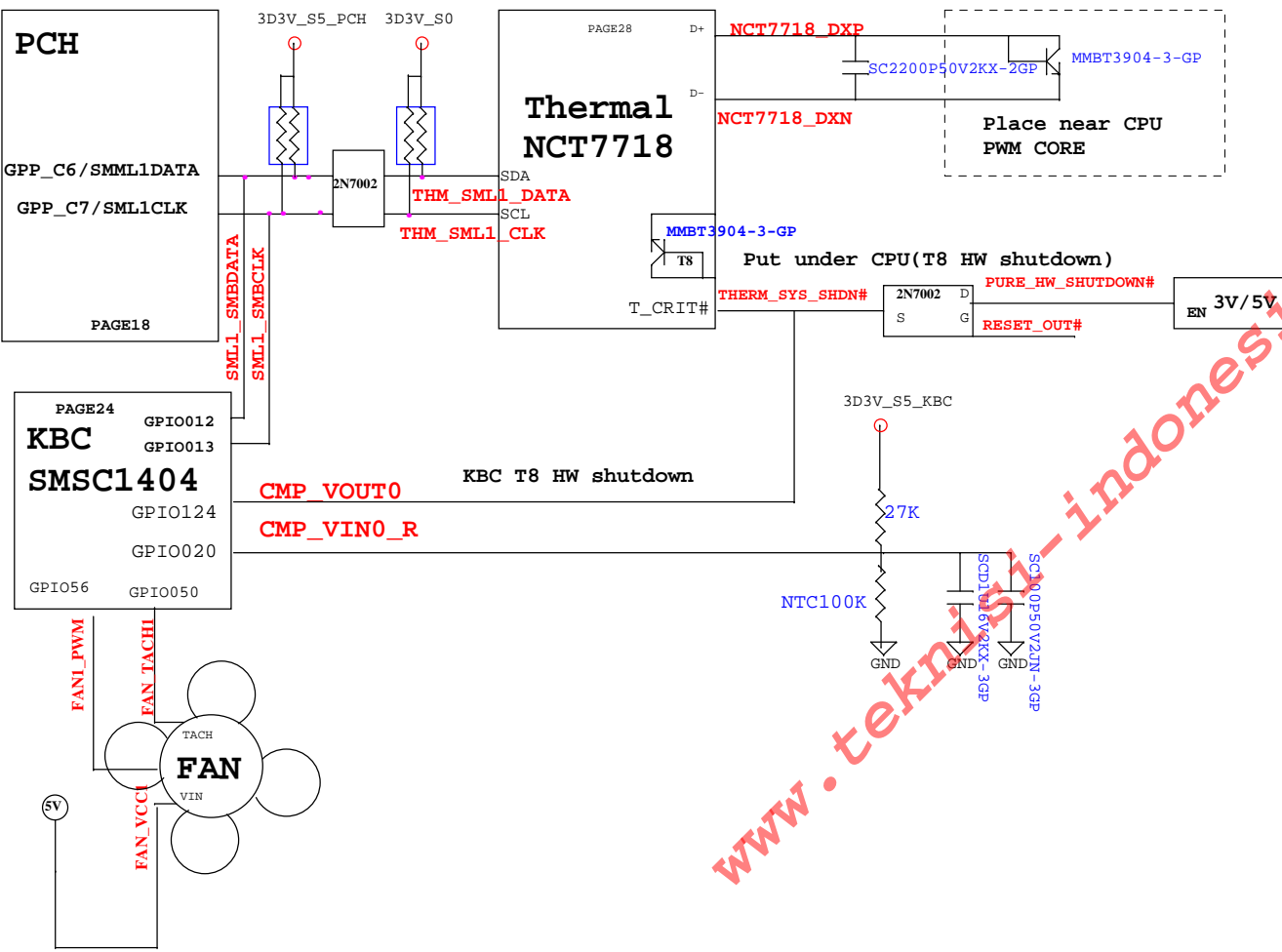


KBC SMBus Block Diagram

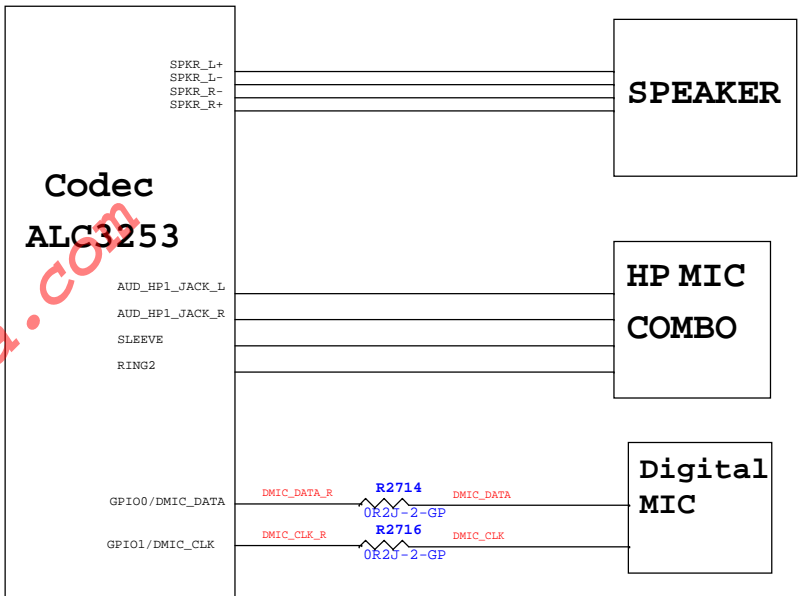


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Thermal Block Diagram



Audio Block Diagram



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